

1	Cover Page
2	Block Diagram
3	SMBUS/CLK/RST Block
4	CPU (CLK,CFG,VID,BPM,DEBUG)
5	CPU (PEG,DMI,DDI,EDP)
6	CPU (DDR4-CHA)
7	CPU (DDR4-CHB)
8	CPU (CPU POWER)
9	CPU(VSS)
10	DDR4 CHA SO-DIMM1
11	DDR4 CHB SO-DIMM2
12	PCH(DMI,PCIE,USB30,USB20)
13	PCH(PCIE,SATA,C LINK,GPIO)
14	PCH(HDA,JATG,SUMBUS,SPI)
15	PCH(DDP,CNV,XDP)
16	PCH(CLK,REQ)
17	PCH(PCH POWER)
18	PCH(I2C,UART,VSS)
19	Blank
20	Strap pin
21	DSW
22	SPI ROM
23	Display Port B
24	Display Port C
25	EXT_CONBTB_USB3/USB2/DP/COM
26	Audio Codec - ALC233VB
27	CEC Modem Standby
28	SIO NCT6686D-L
29	COM Port
30	TPM - TCG 2.0
31	LAN - Jacksonville_i219LM
32	RJ45
33	Rear USB3 with ODD/Debug
34	Rear USB3 x 2
35	Front USB3 Charger x1
36	Front Type-C RTS5449E
37	M.2 2230-E WIFI/ BT/CNV
38	M.2 2280-M SSD-2-BLACK
39	M.2 2280-M SSD-1-WHITE
40	Sata FFC
41	PWRGD & Bleed Off
42	PCIEX8
43	XDP
44	FP-Button
45	eSIO-Thermal Sensing
46	EXT_CON-TBT
47	APS
48	Hole/PCB/Virtual symbol
49	PWR-Power Diagram
50	PWR-DC_IN/ RTC Battery
51	PWR-IMVP8-ON_NCP81220
52	PWR-IMVP8-CPU_VCCIA
53	PWR-IMVP8-VCCGT
54	PWR-IMVP8-VCCSA
55	PWR-VCCIO
56	PWR-3V/5V
57	PWR-VDIMM
58	PWR-1V05_PCH/1V8_S5
59	PWR-12V_PCIE
60	POWER Sequence(G3-S0)
61	GPIO table
62	FAN CRTL
63	PWRLED/HDDLLED
64	M.2 3042-B LTE 5G

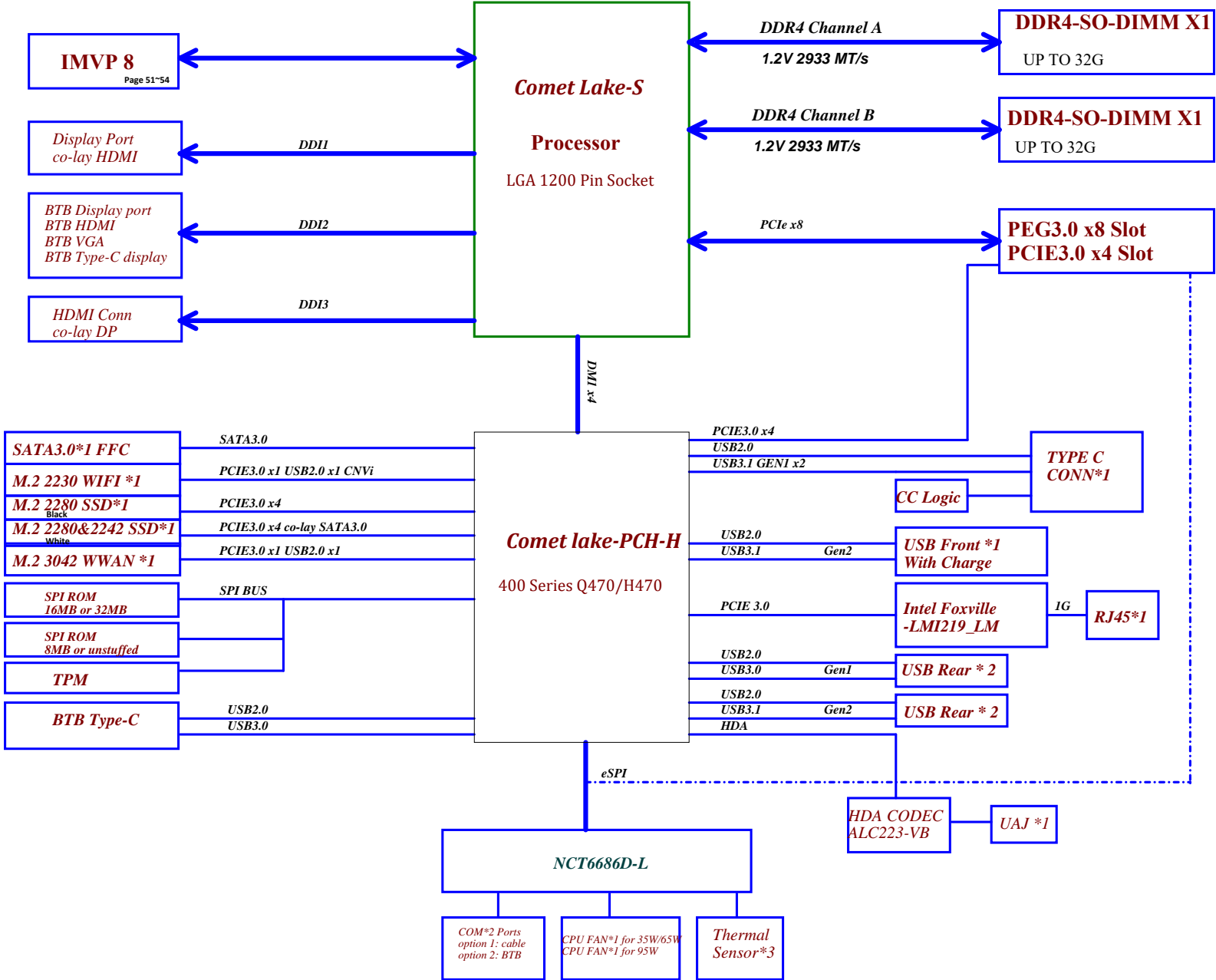
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Tiny6 GH470 MB Schematics Document Intel Comlet Lake-S CPU+Comlet Lake-H PCH

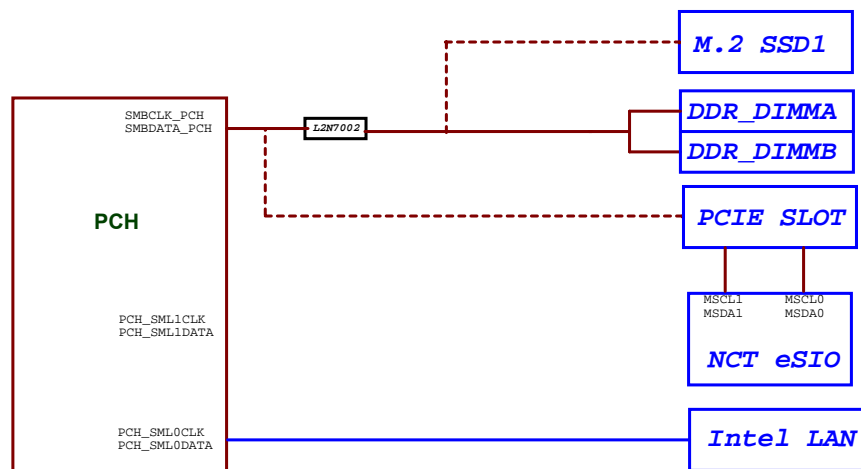
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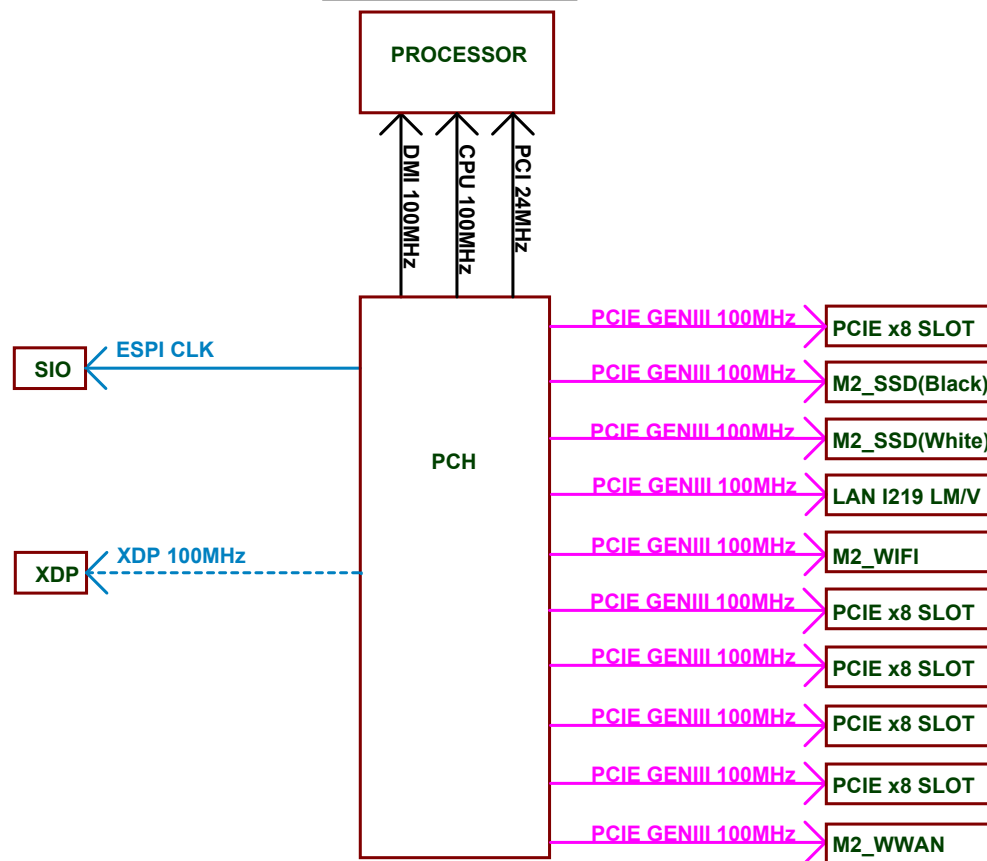
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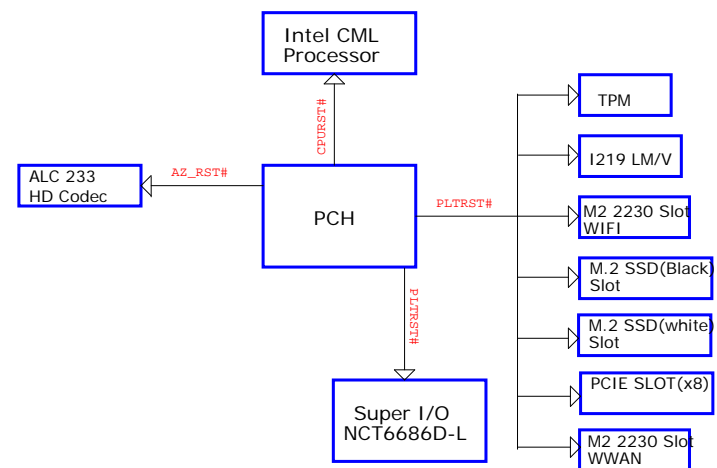
SMBUS Block Diagram




CLOCK MAP



RESET MAP



BOM Structure	BTO Item
@	Not stuff
Q490@	For Q490 SKU (M90Q,M80Q,NEC Q490,WS Tiny), 32M SPI ROM
H470@	For H470 SKU
DEBUG@	For NPI debug need
BMC@	For BMC part
DPI@	For 1st DP colay HDMI port, DP SKU part
DP2@	For 2nd DP colay HDMI port, DP SKU part
HDMI1@	For 1st DP colay HDMI port, HDMI SKU part
HDMI2@	For 2nd DP colay HDMI port, HDMI SKU part
EMC@	For EMC part
EMC_NS@	For EMC nu-stuff part
PCIEX8X4@	For PCIE X8/X4 part
SYSFAN@	For System FAN part-only reserved
MS@	For Modern Standby function
SSD2@	For M.2 SSD(Black) PCIE part, only M920X(Q370) need
M2_EXP@	For M.2 SSD(White) docking function need
ME@	For ME part
DOTLED@	For NEC DOT LED remove
HDMILOGO@	HDMI LOGO
BATTERY@	Battery cell
SPIROM@	For 45J SPI ROM

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Date: Monday, March 28, 2020				[Sheet 3 of 84]			

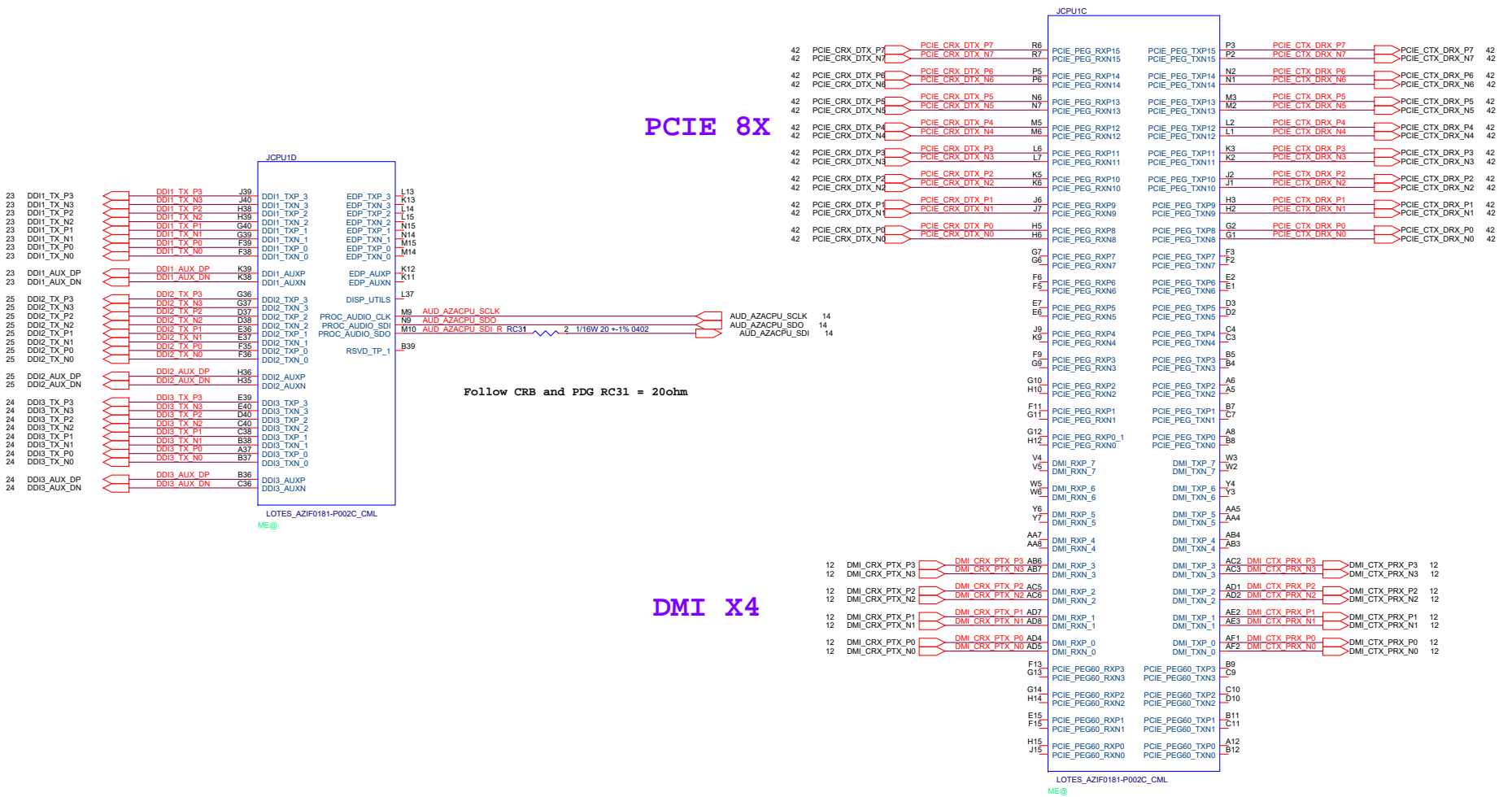
DDI1_DP1

DDI2_BTBT

DDI3_DP2

PCIE 8X

DMI X4



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				Document Number	1.0
				GH470	
				Date	Monday, March 23, 2020
				Sheet	5 of 84

SO-DIMM DDR4 CHA

The diagram illustrates the electrical connections for an SO-DIMM DDR4 CHA module. It shows the interface between the JCPU1A connector, the DDR4 memory array (N1L), and various control and data signals. Key components include:

- JCPU1A:** The main system connector at the top.
- DDR4 (ILYDDR4) N1L:** The memory array located in the center.
- Data Bus:** Connections for DDRA_DQ[0..63] and related signals.
- Control Signals:** Includes DDRA_CLK1, DDRA_CKE1, DDRA_CS#1, DDRA_ODT1, DDRA_BA1, DDRA_BG1, DDRA_MA16_RAS#, DDRA_MA15_CAS#, DDRA_MA14_WE#, DDRA_ACT#, DDRA_PAR, and DDRA_ALERT#.
- Error Correction Code (ECC):** Connections for DDRA_ECC[0..7].
- Voltage Reference:** DDRA_VREF_CA and DDRA_VREF_CA0.

Security Classification

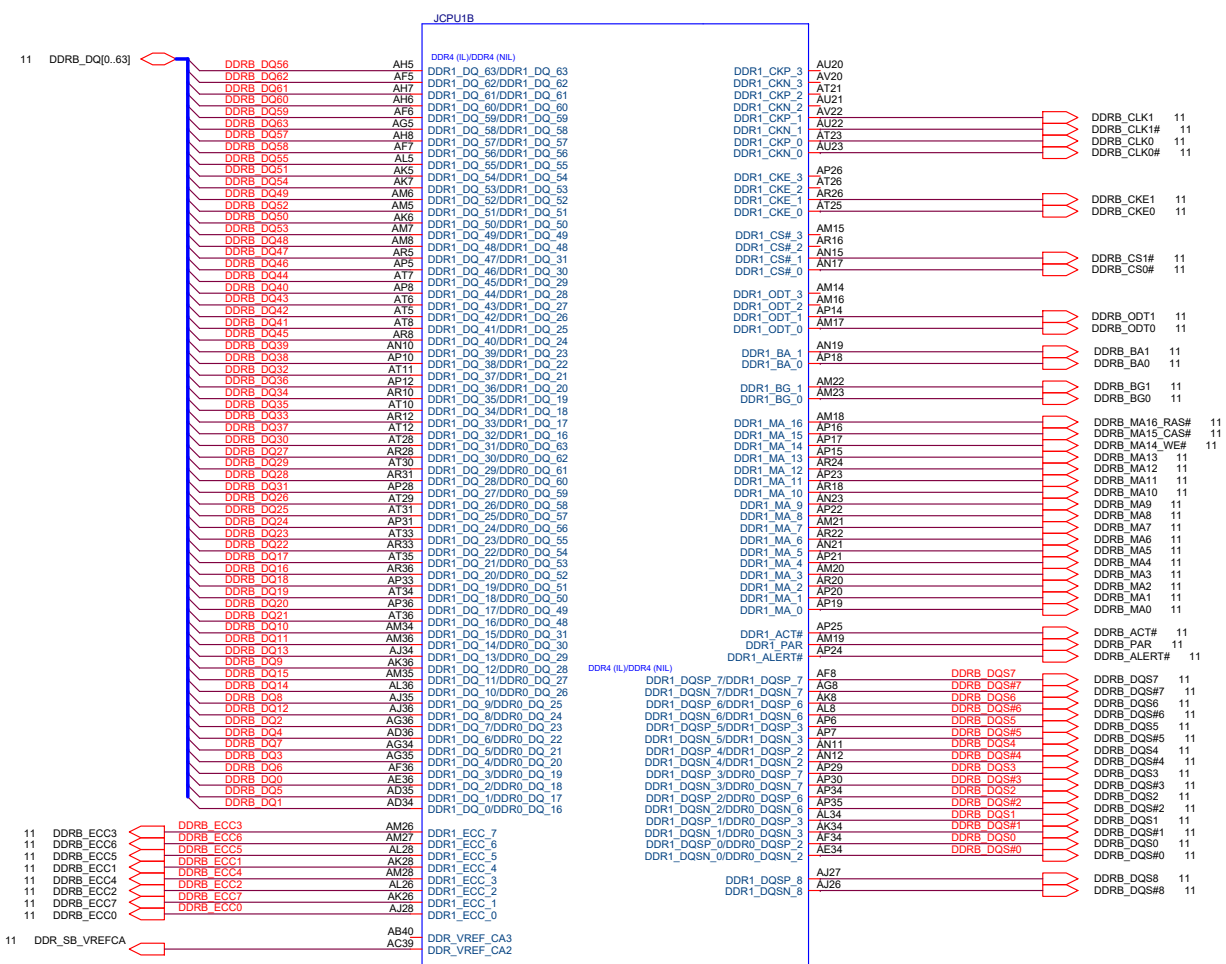
Security Classification	Title
LC Future Center Secret Data	CPU (DDR4-CHA)


Issued Date: 2015/08/20
Deciphered Date: 2016/08/20

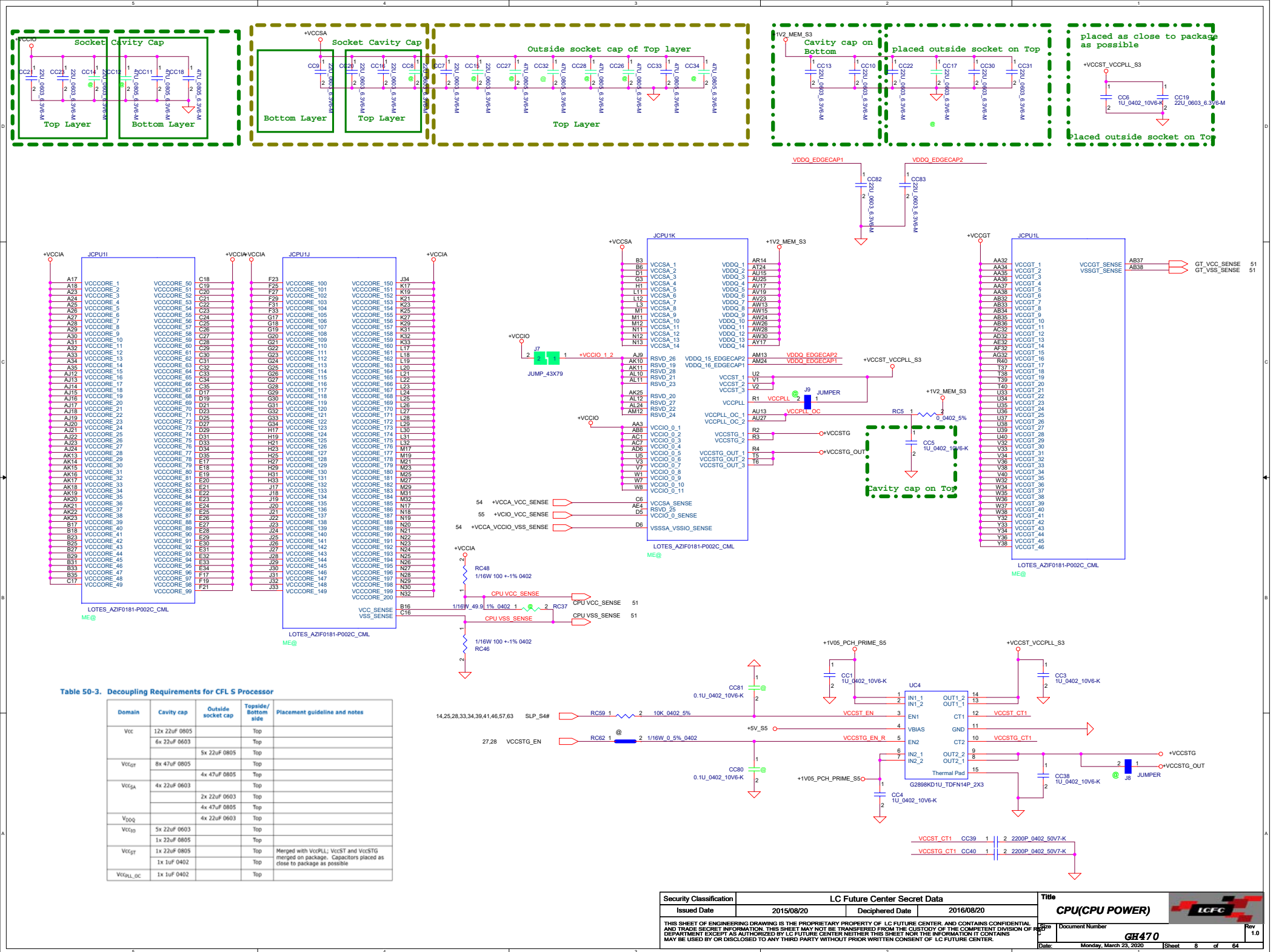
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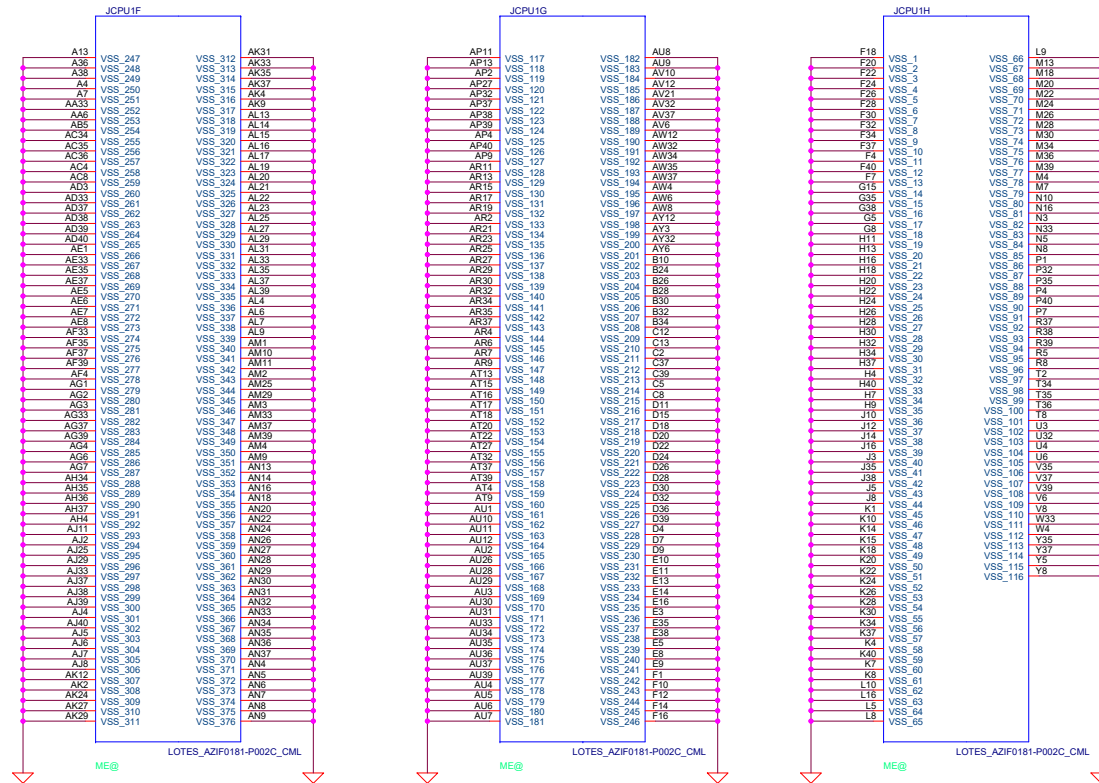
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Sheet: 6 of 64
Rev: 1.0

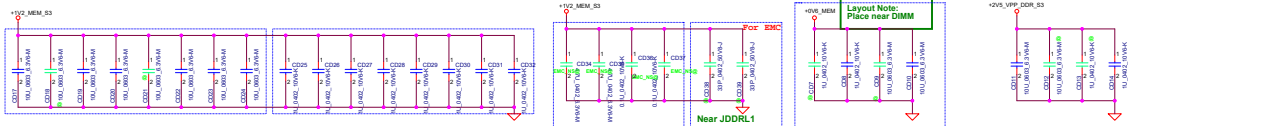
SO-DIMM DDR4 CHB



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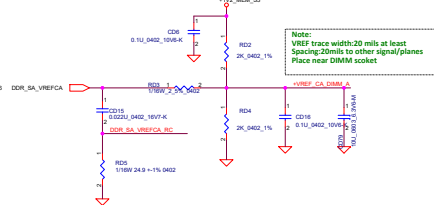
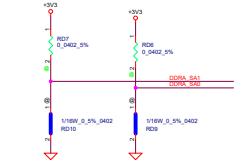
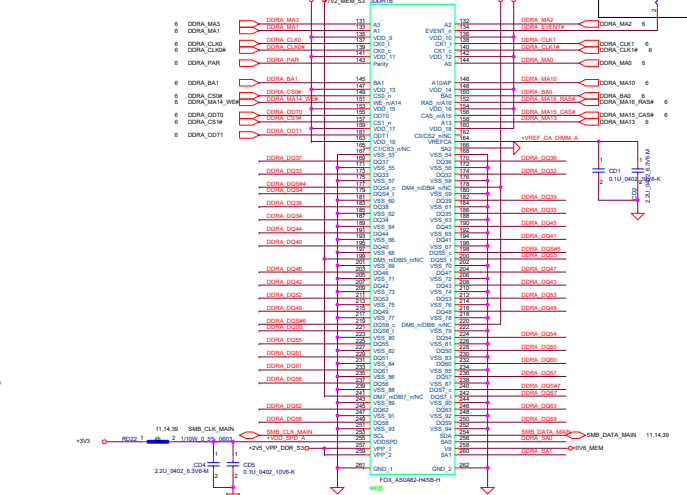
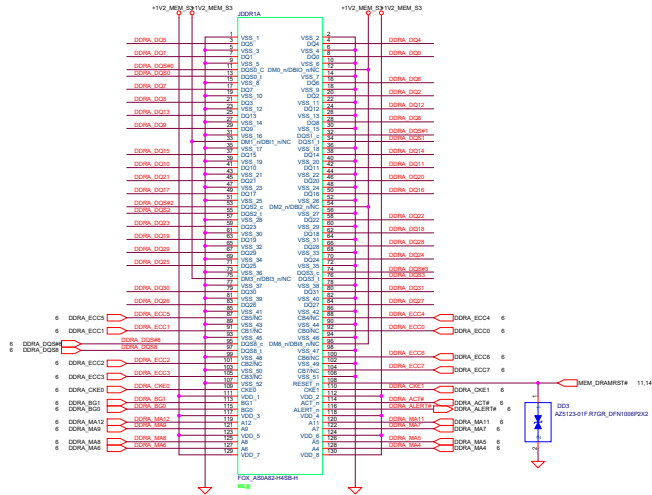


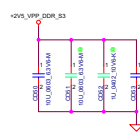
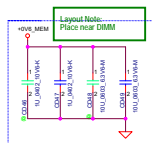
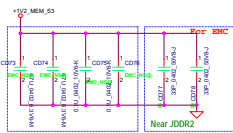
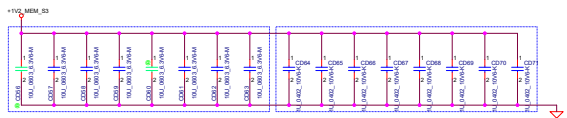




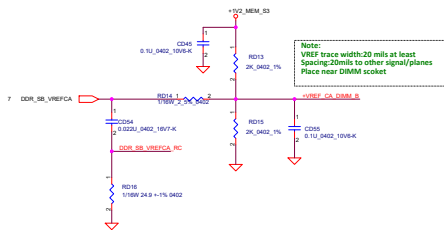
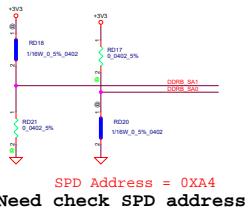
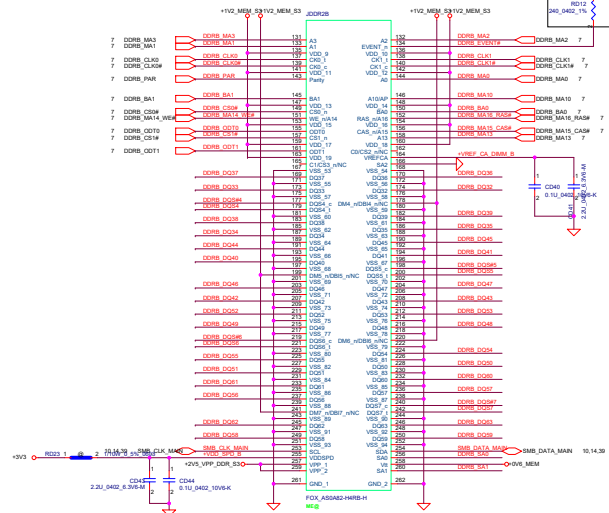
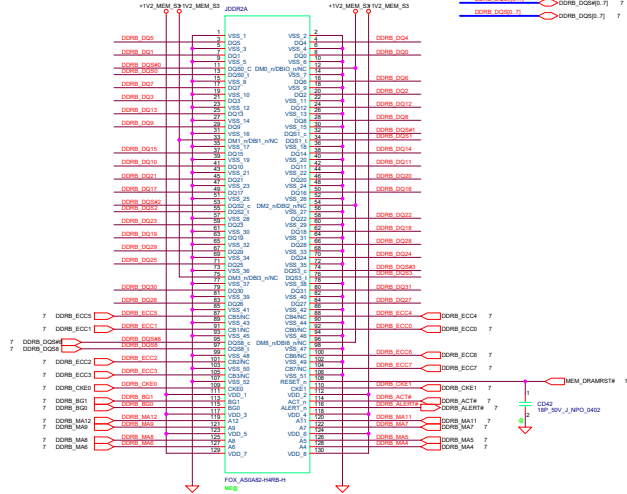
Silkscreen*
DIMM1

DDR4_DQ0[0] DDR4_DQ0[0] 6
DDR4_DQ0[1] DDR4_DQ0[1] 6
DDR4_DQ0[2] DDR4_DQ0[2] 6
DDR4_DQ0[3] DDR4_DQ0[3] 6

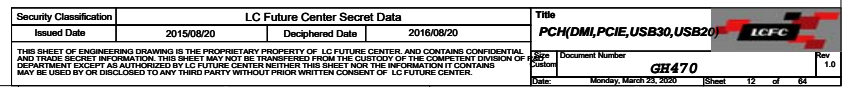


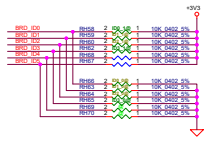


DDR4 SO-DIMM SilkScreen® DIMM2



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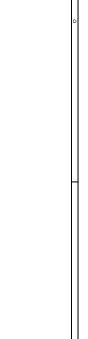
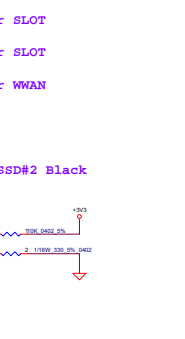
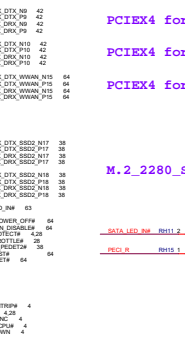
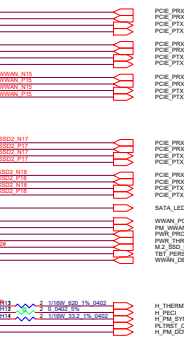
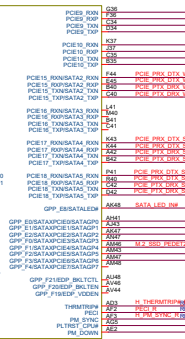
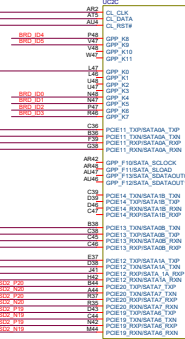
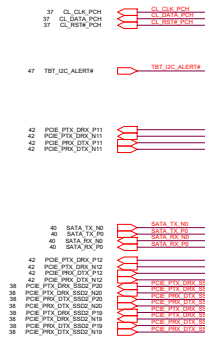


PCIEX4 for SLOT

SATA FFC Cable

PCIEX4 for SLOT

M.2_2280_SSD#2 Black



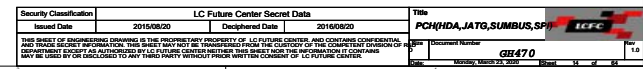
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	Board ID MAP				ID5	ID4	ID3	ID2	ID1	ID0
Tiny6	P340 Workstation	Q470	Corp		1	1	0	0	0	0
	M90q Li	Q470	Corp		1	1	0	0	0	1
	M80q Li	Q470	Corp		1	1	0	0	1	0
	M80q LC	Q470	Corp		1	1	0	0	1	1
	M70q Li	H470	Consumer		1	1	0	1	0	0
	M70q LC	H470	Consumer		1	1	0	1	0	1
	NEC M80q	Q470	Corp		1	1	0	1	1	0
	NEC M70q	H470	Consumer		1	1	0	1	1	1
	Tiny H550Q consumer	H470	Consumer		1	1	1	0	0	0
	Tiny Server	W480	Corp		1	1	1	0	0	1
	Tiny AIO V70	H470	Consumer		1	1	1	0	1	0
	Tiny Amazon	H470	Consumer		1	1	1	0	1	1

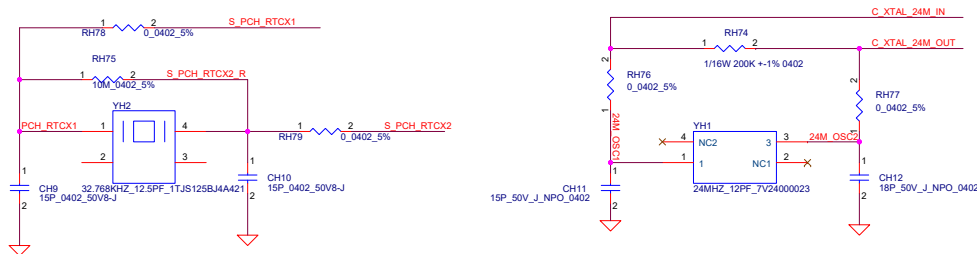
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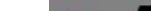
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6	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)
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8	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)
9	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)	PCIe/USB 3.2 Gen 1x1 (5 Gb/s)
10	PCIe*,GfE	PCIe*,GfE	PCIe*,GfE	PCIe*,GfE	PCIe*,GfE	PCIe*,GfE	PCIe*,GfE	PCIe*,GfE	PCIe*,GfE
11	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*
12	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*
13	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*
14	PCIe*,GfE	PCIe*,GfE	PCIe*,GfE	PCIe*,GfE	PCIe*,GfE	PCIe*,GfE	PCIe*,GfE	PCIe*,GfE	PCIe*,GfE
15	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*
16	PCIe*,SATA 0A	PCIe*,SATA 0A	PCIe*,SATA 0A	PCIe*,SATA 0A	PCIe*,SATA 0A	PCIe*,SATA 0A	PCIe*,SATA 0A	PCIe*,SATA 0A	PCIe*,SATA 0A
17	SATA 1A/PCIe*,GfE	SATA 1A/PCIe*,GfE	SATA 1A/PCIe*,GfE	SATA 1A/PCIe*,GfE	SATA 1A/PCIe*,GfE	SATA 1A/PCIe*,GfE	SATA 1A/PCIe*,GfE	SATA 1A/PCIe*,GfE	SATA 1A/PCIe*,GfE
18	SATA 0B/PCIe*,GfE	SATA 0B/PCIe*,GfE	SATA 0B/PCIe*,GfE	SATA 0B/PCIe*,GfE	SATA 0B/PCIe*,GfE	SATA 0B/PCIe*,GfE	SATA 0B/PCIe*,GfE	SATA 0B/PCIe*,GfE	SATA 0B/PCIe*,GfE
19	SATA 1B/PCIe*	SATA 1B/PCIe*	SATA 1B/PCIe*	SATA 1B/PCIe*	SATA 1B/PCIe*	SATA 1B/PCIe*	SATA 1B/PCIe*	SATA 1B/PCIe*	SATA 1B/PCIe*
20	SATA 2/PCIe*	SATA 2/PCIe*	SATA 2/PCIe*	SATA 2/PCIe*	SATA 2/PCIe*	SATA 2/PCIe*	SATA 2/PCIe*	SATA 2/PCIe*	SATA 2/PCIe*
21	SATA 3/PCIe*	SATA 3/PCIe*	SATA 3/PCIe*	SATA 3/PCIe*	SATA 3/PCIe*	SATA 3/PCIe*	SATA 3/PCIe*	SATA 3/PCIe*	SATA 3/PCIe*
22	SATA 4/PCIe*	SATA 4/PCIe*	SATA 4/PCIe*	SATA 4/PCIe*	SATA 4/PCIe*	SATA 4/PCIe*	SATA 4/PCIe*	SATA 4/PCIe*	SATA 4/PCIe*
23	SATA 5/PCIe*	SATA 5/PCIe*	SATA 5/PCIe*	SATA 5/PCIe*	SATA 5/PCIe*	SATA 5/PCIe*	SATA 5/PCIe*	SATA 5/PCIe*	SATA 5/PCIe*
24	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*
25	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*
26	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*
27	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*
28	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*
29	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*	PCIe*

Figure 3-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H

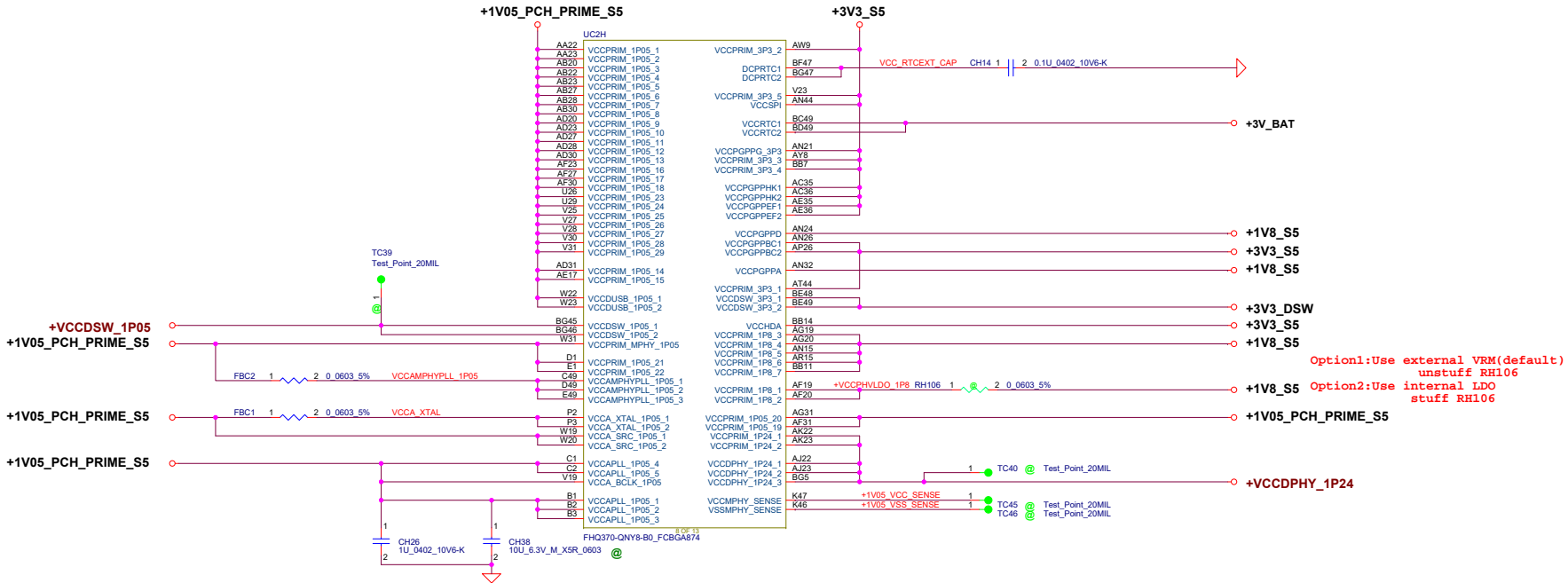
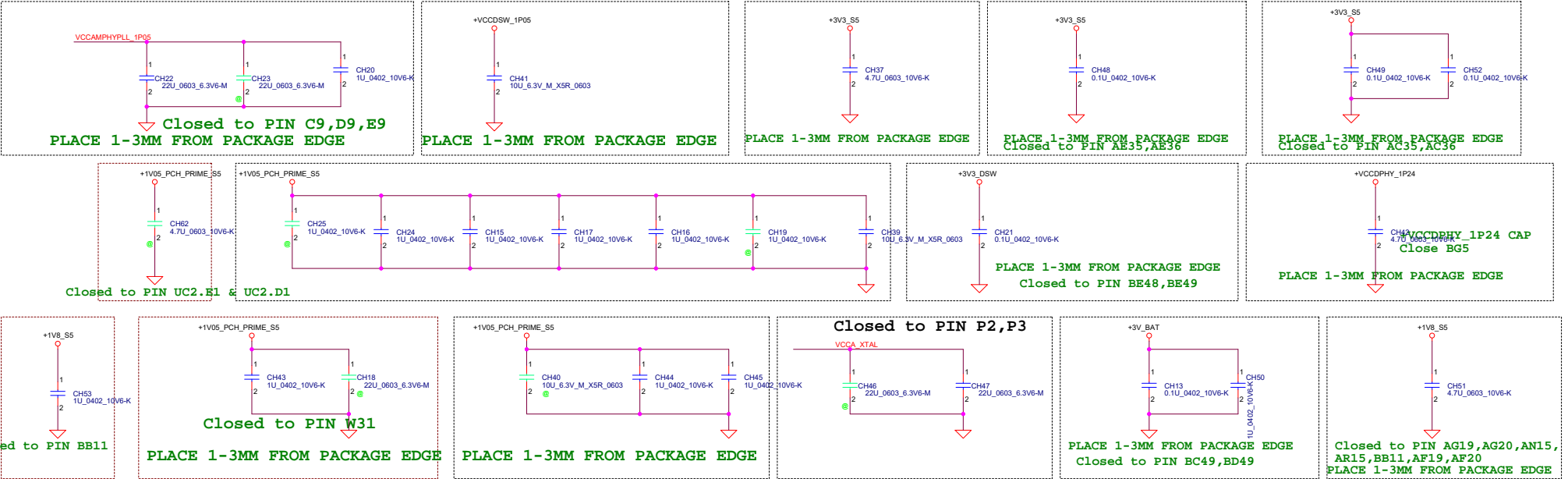
Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1 #7	USB3.1 Gen1 #8	USB3.1 Gen1 #9	USB3.1 Gen1 #10	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	SATA 1a	SATA 0b	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
							PCIe* #1												GbE												
Intel® RST Support																															

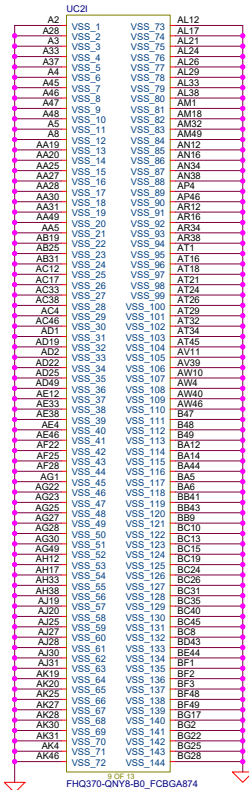




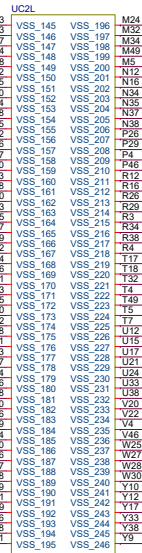
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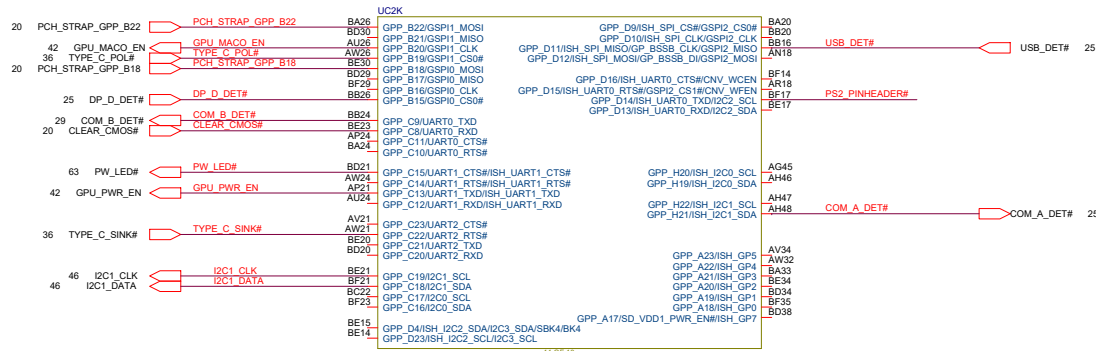




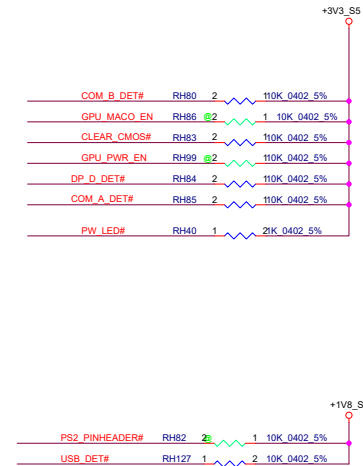
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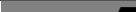


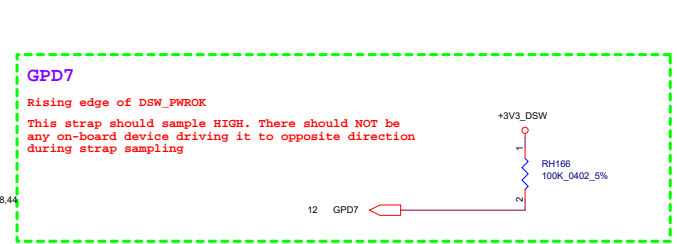
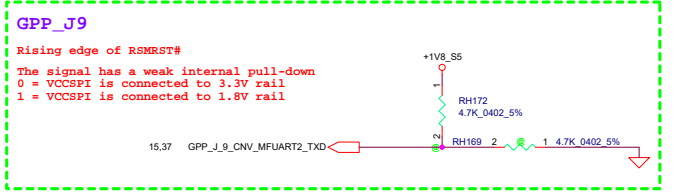
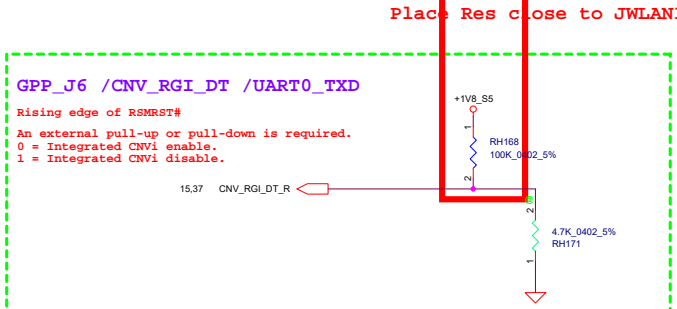
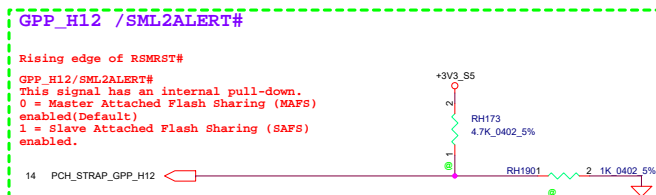
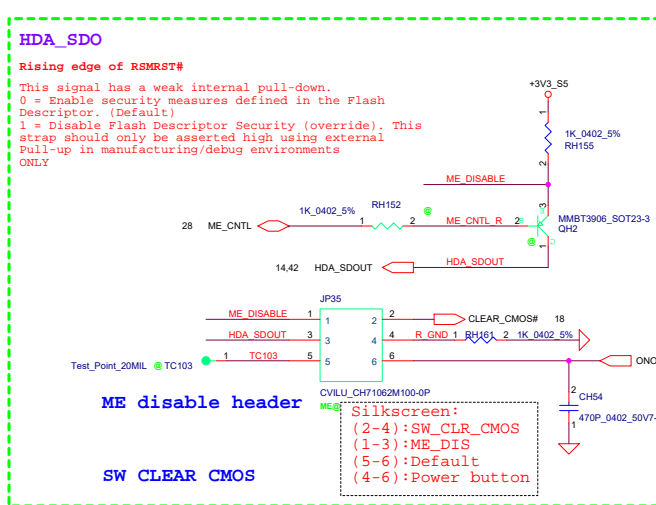
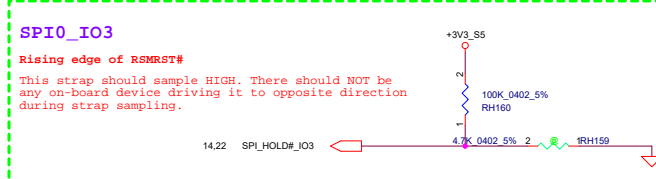
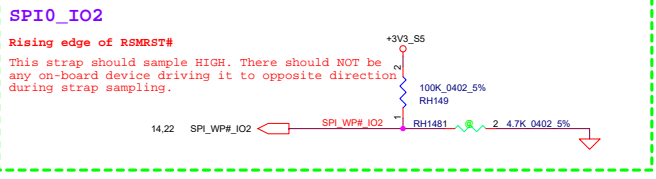
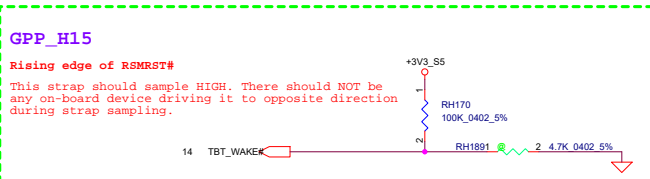
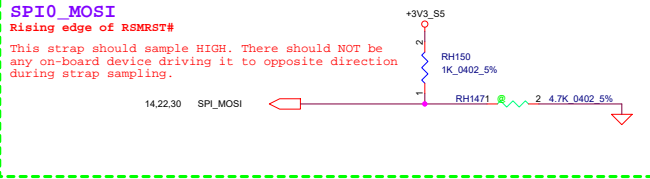
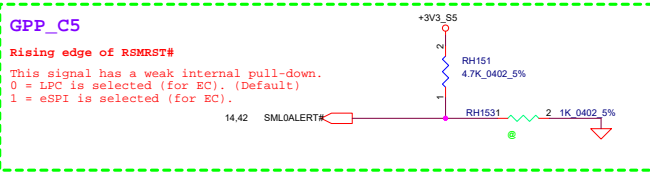
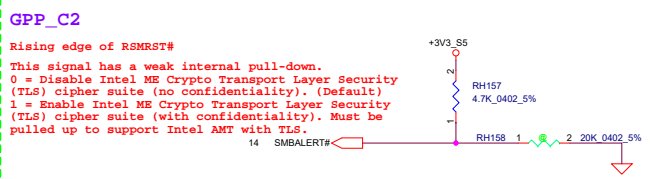
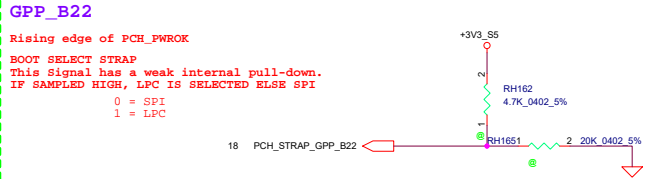
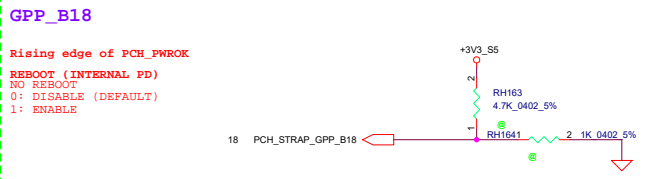
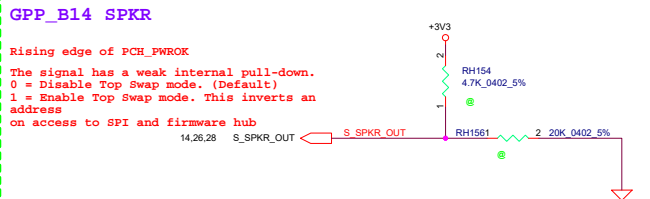
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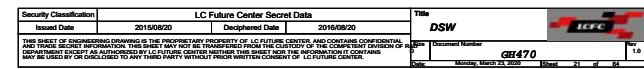


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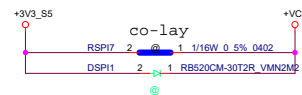
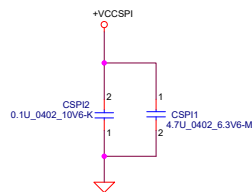


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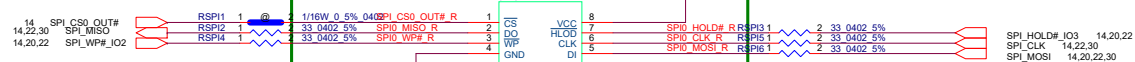




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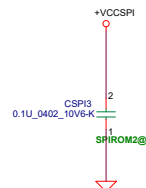


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14.22.30 SPI_MISO
14.20.22 SPI_WP#_JO2

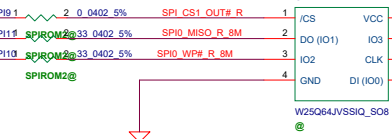


Colay with JBIOS1

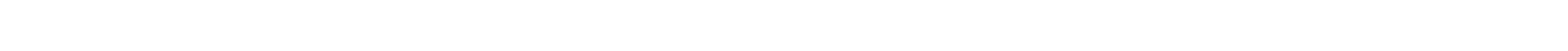
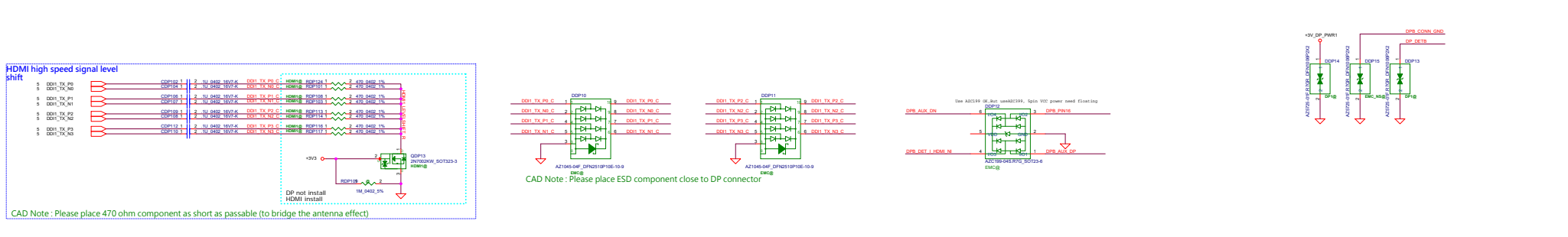
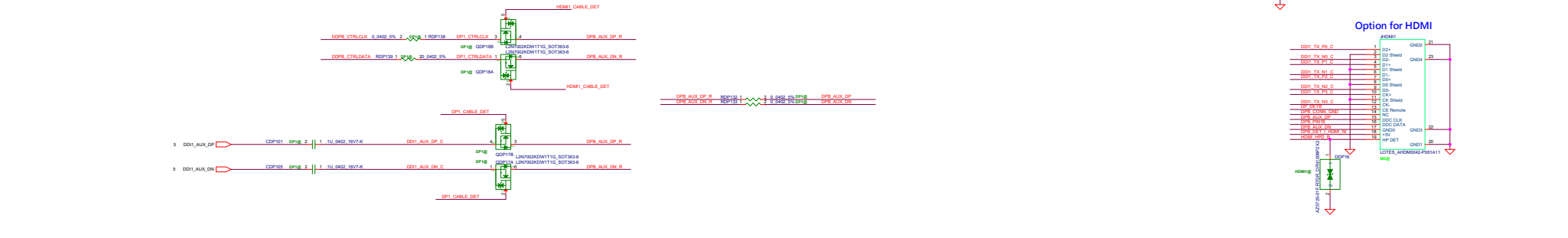
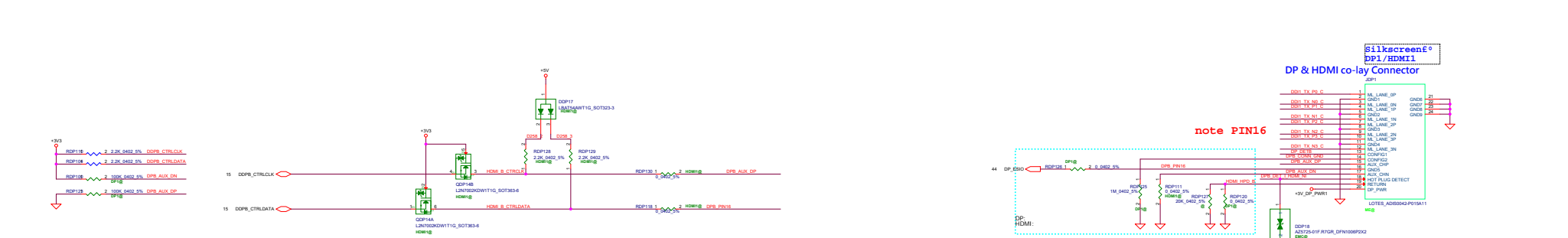
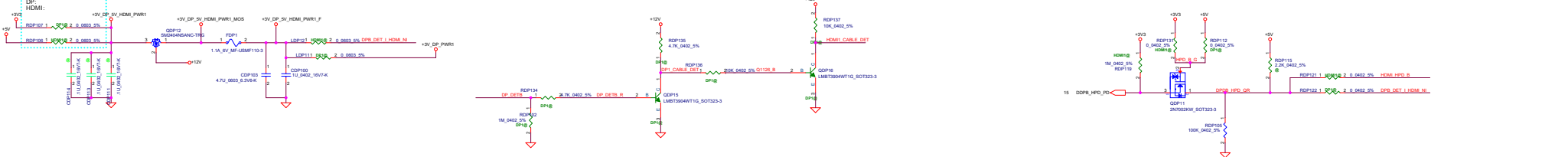
8M ROM

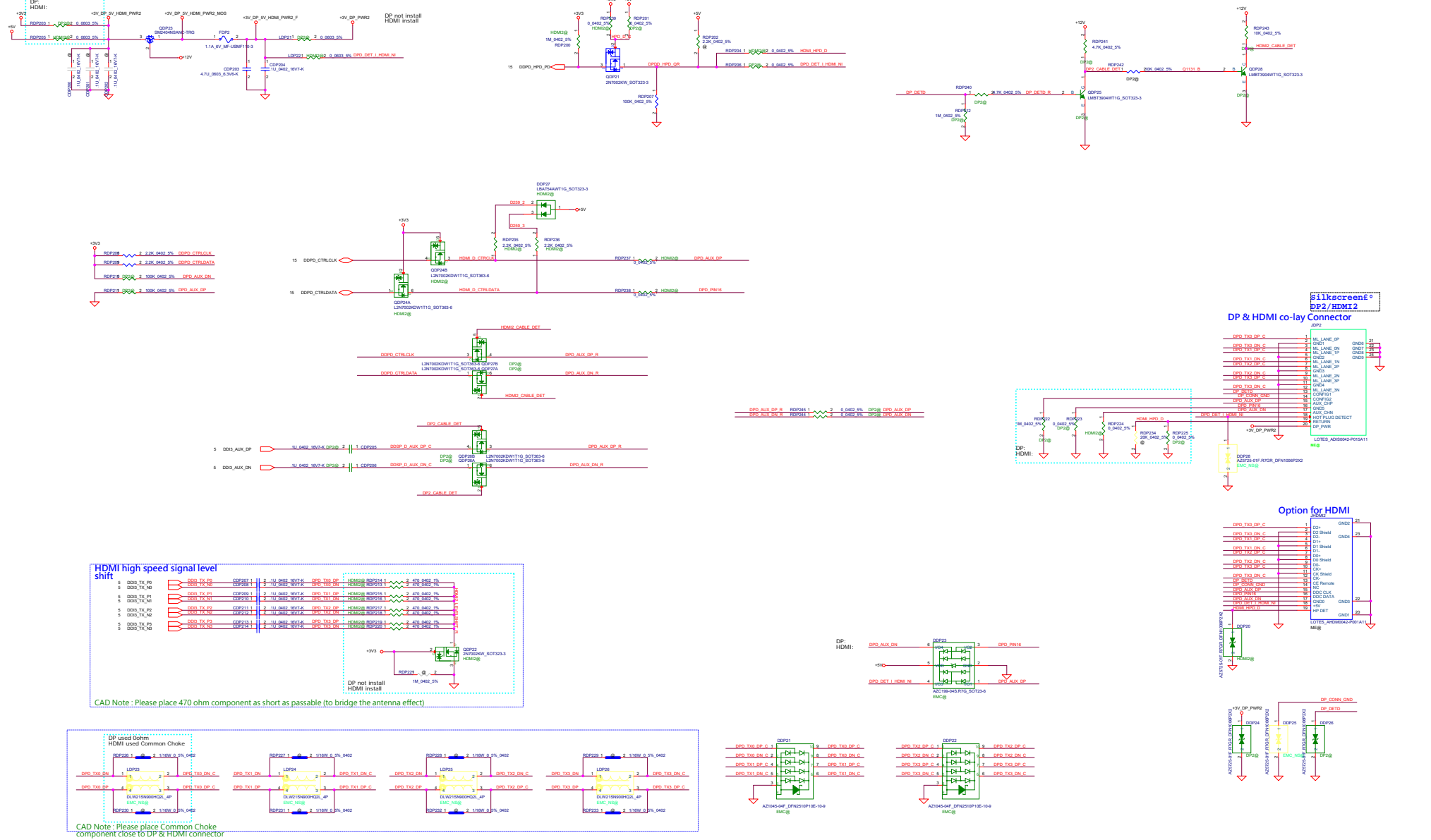


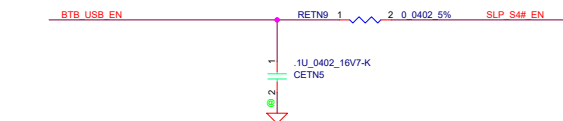
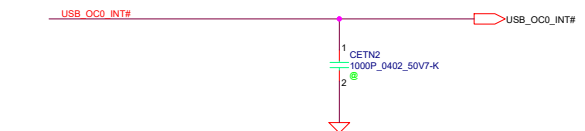
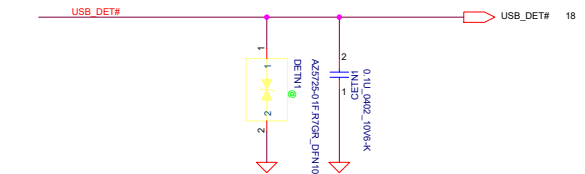
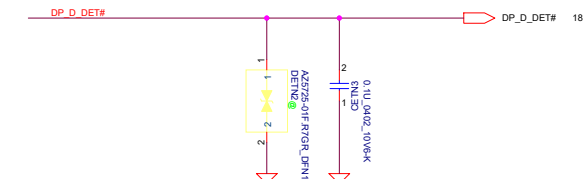
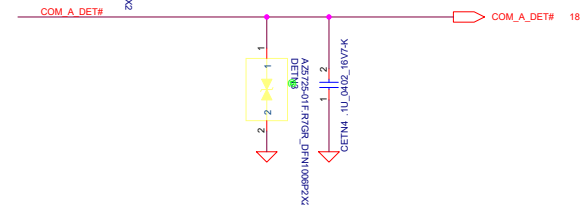
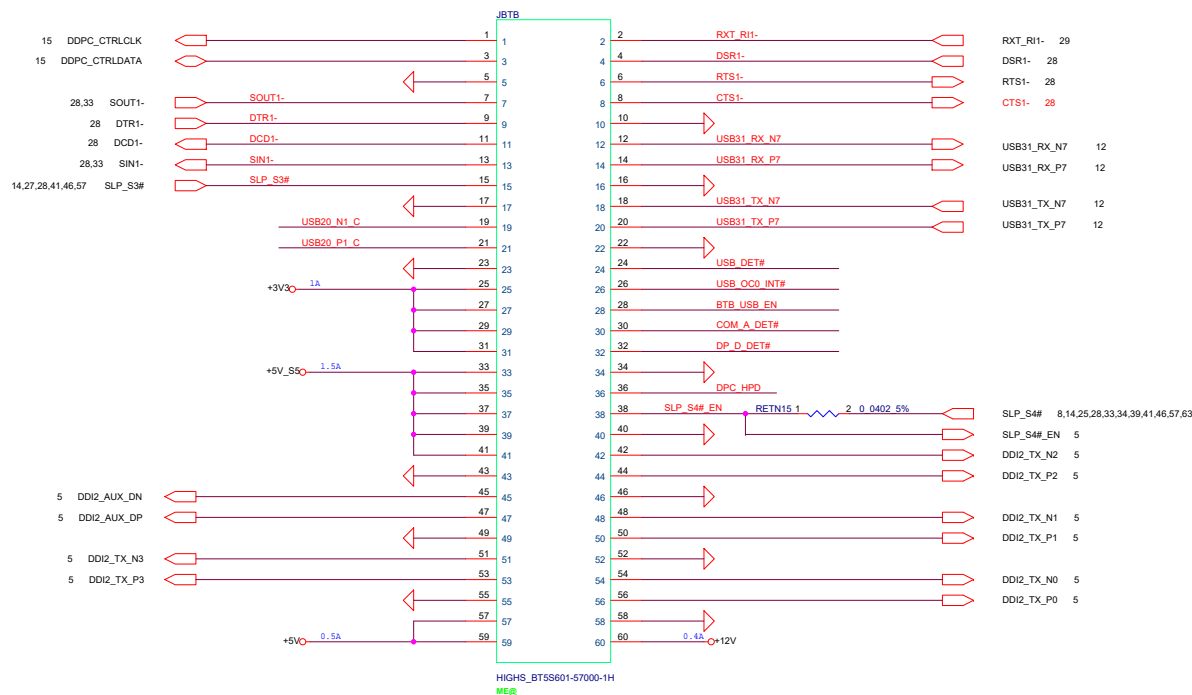
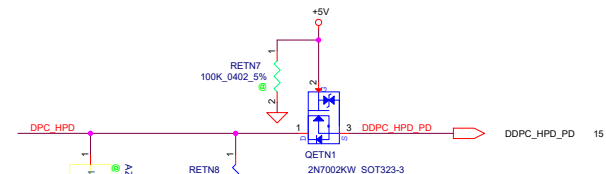
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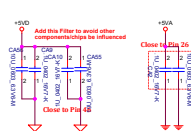
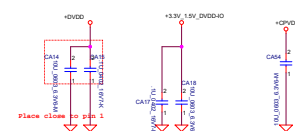
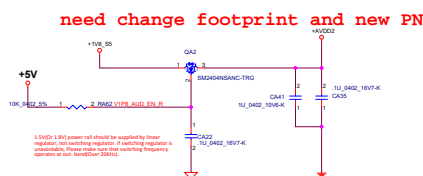
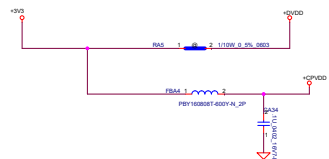
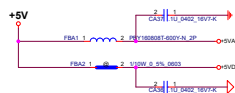


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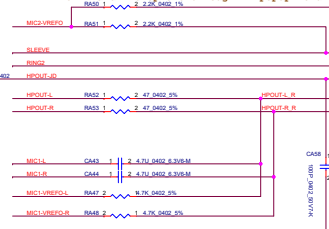






ALC233-VA ID1 10K, ID2 39.2K,
ALC233-VB ID1 100K, ID2 200K

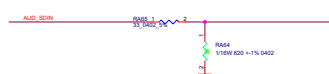
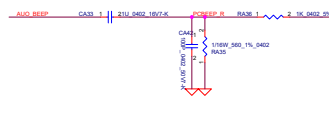
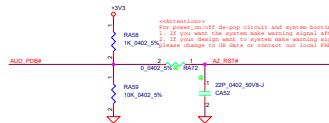
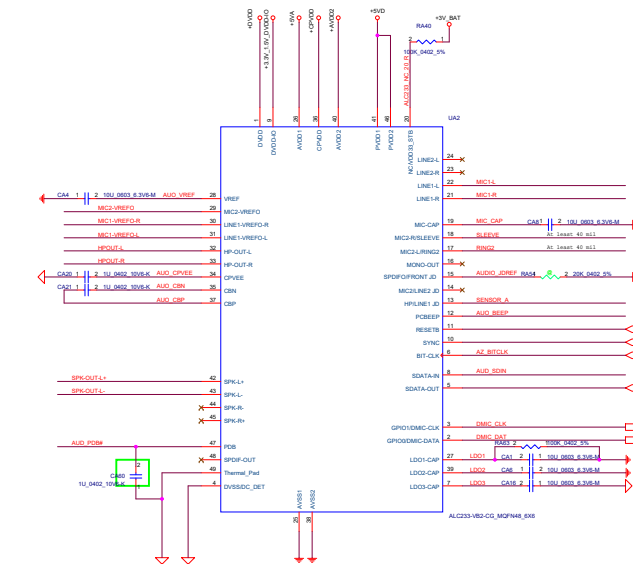
Supported iPhone/Nokia headset, Headphone,
Line-In and Microphone through SW popup menu



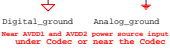
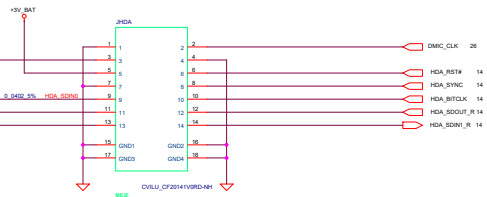
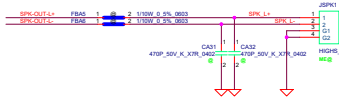
FB1/FB2 should choose DC resistance (Rdc) < 30m-ohm
to get the best audio performance for SP connections

Silkscreen®
DAJ

Audio Jack (C0800) (JA141)

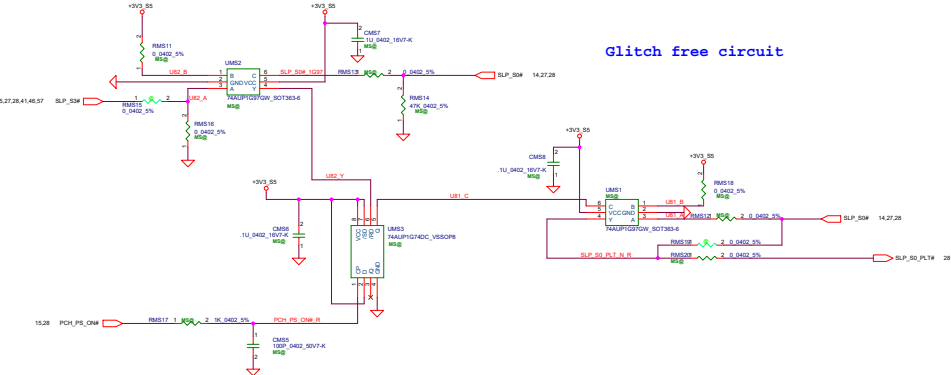


Silkscreen®
SPKR

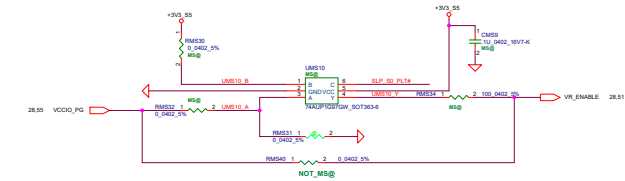


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				CH470
				Version
				1.0

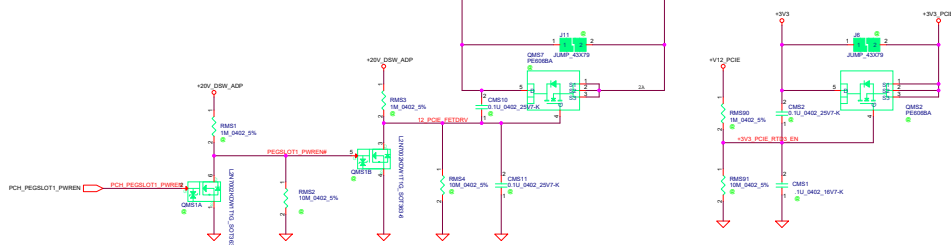
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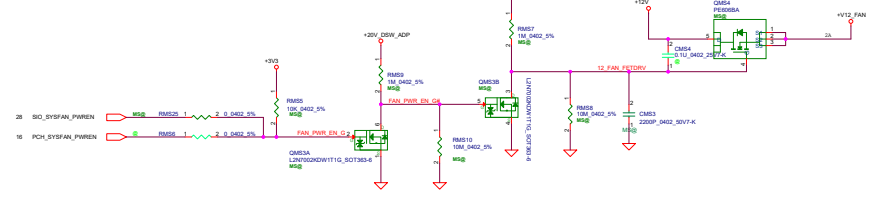
Mask circuit for VR_ENABLE



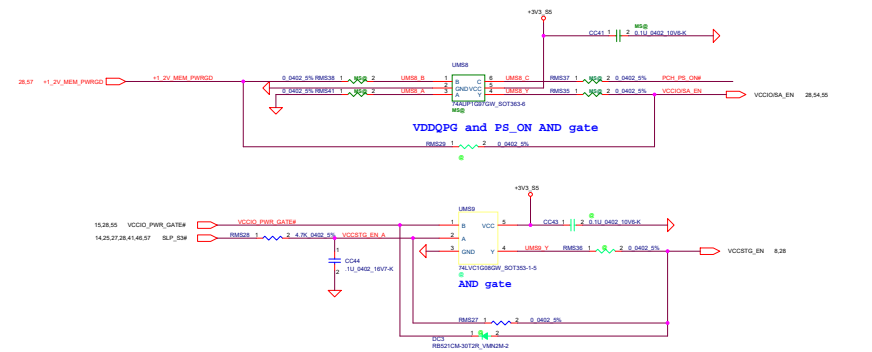
V3.3S PCIE SLOT GENERATION



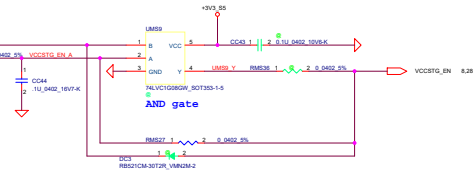
FOR FAN

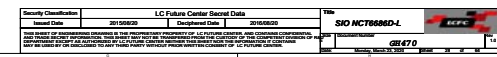


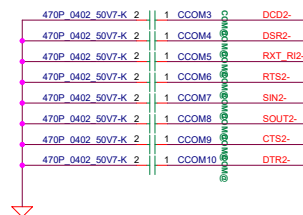
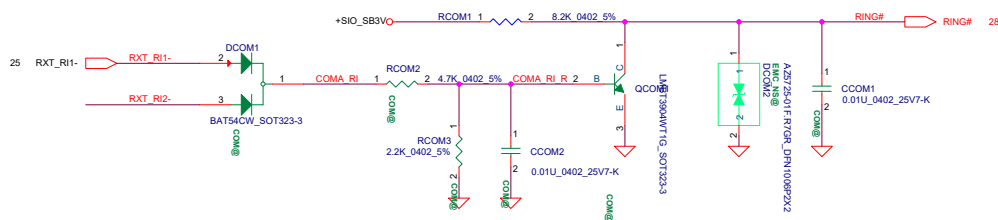
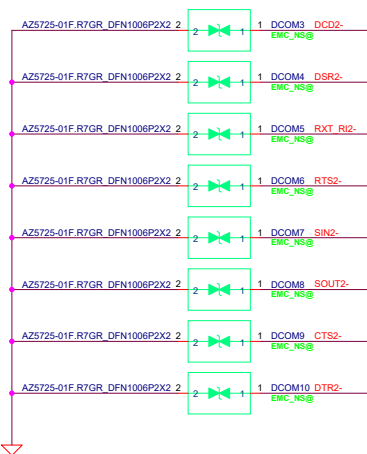
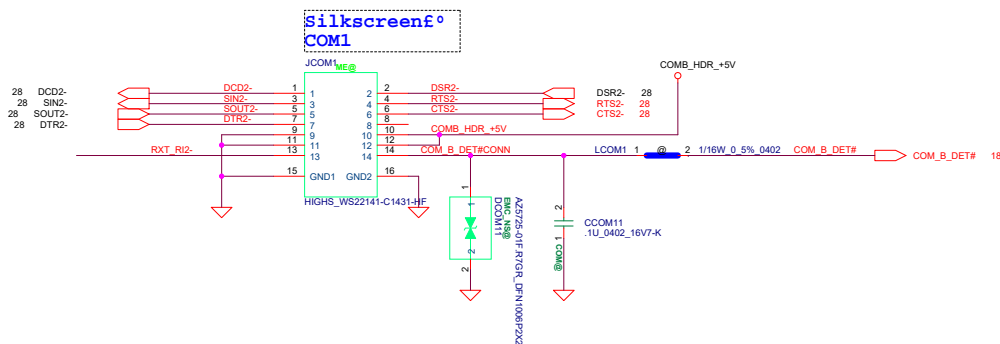
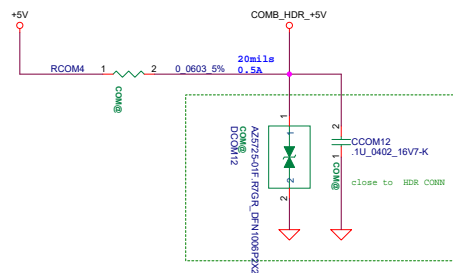
VDDQPG and PS_ON AND gate

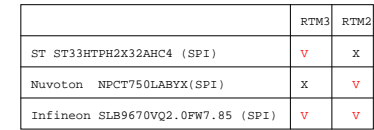



AND gate





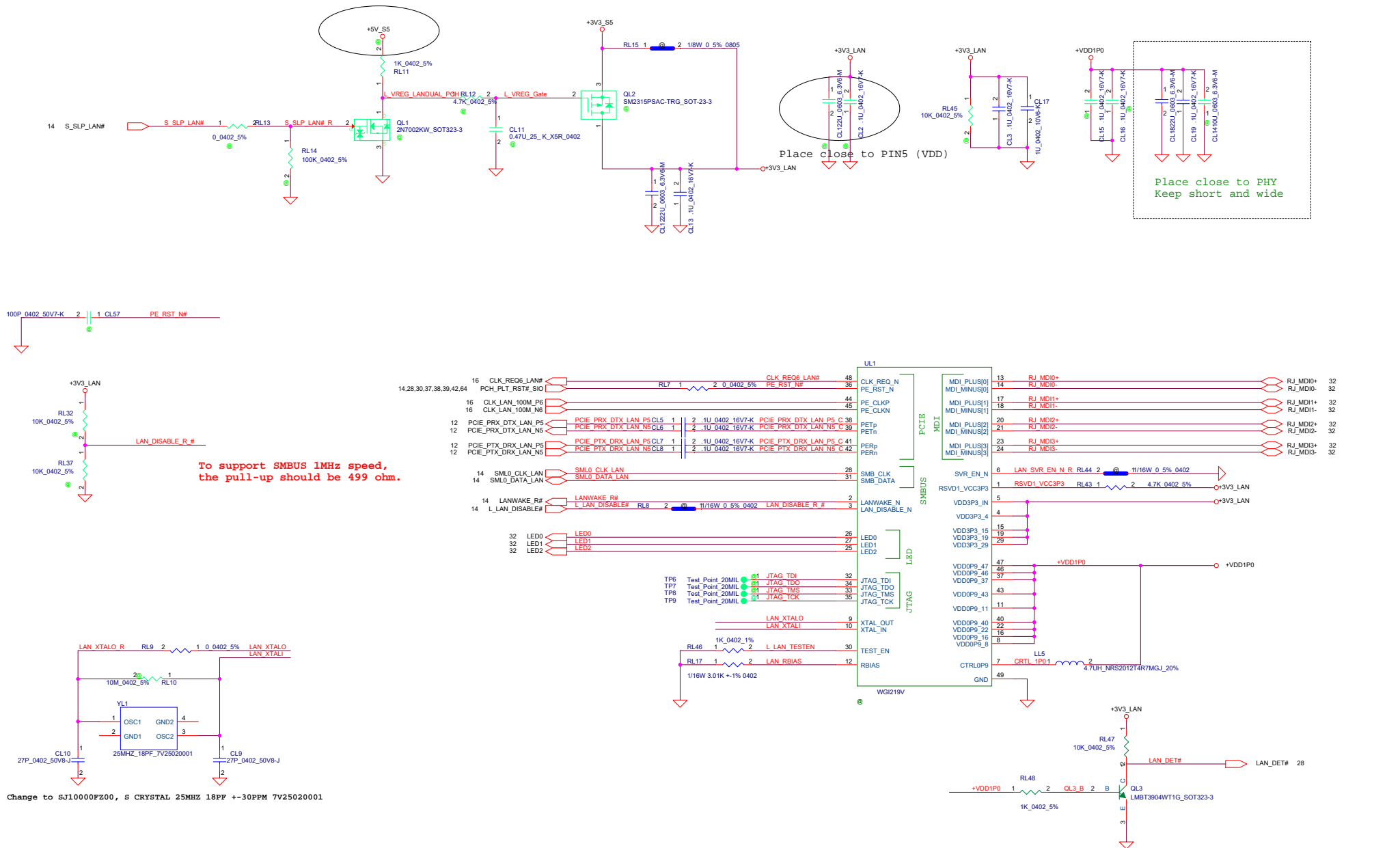


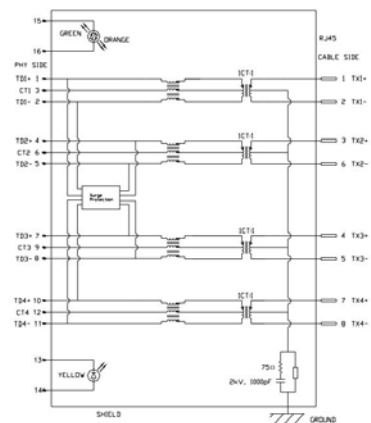


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Issued Date		Deciphered Date		TPM - TCG 2.0			
2015/08/20		2016/08/20					
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				Date: Monday, March 23, 2020		Sheet 30 of 64	

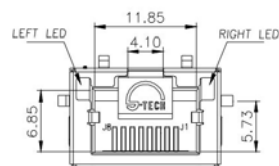
POWER DESIGN NOTE:

> +3.3V_LAN should always have power during all networking conditions (S0, Sx, DeepSx states, WOL, etc.)

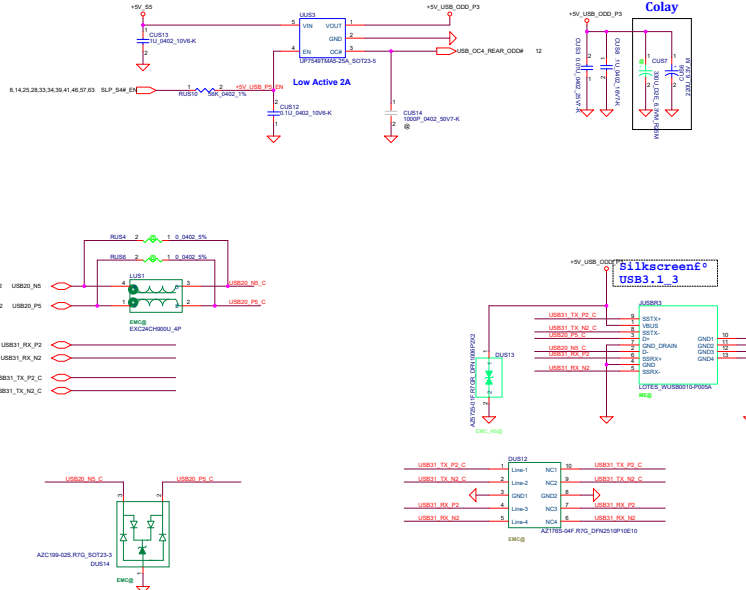




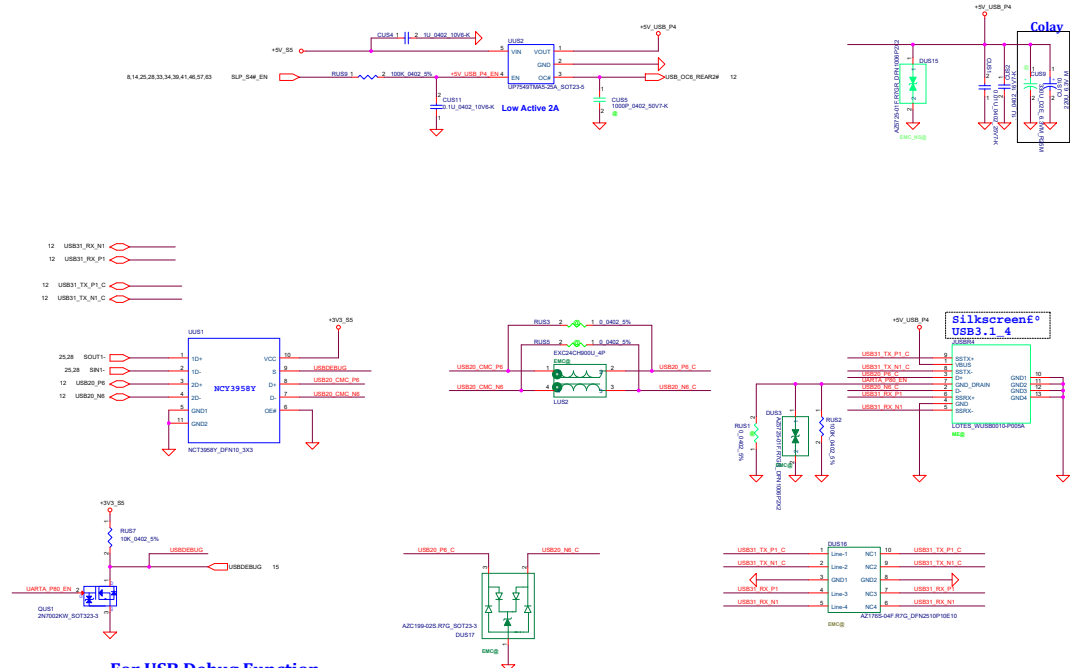
WOL	Status	Yellow	Green	Orange
Don't Care	Off	Off	Off	Off
Off	E3/84/E5	Off	Off	Off
On	10M Inactive	On	Off	Off
On	10M Active	Blinking	Off	Off
On	10M Inactive	On	On	Off
On	10M Active	Blinking	On	Off
On	10B Inactive	On	Off	On
On	10B Active	Blinking	Off	On



Rear Side USB ODD



Rear Side USB 3.1 GEN UART USB debug port




For USB Debug Function

USBDEBUG	Kernel debug
Set input	Set input
Get outputmask Low	Get outputmask

UARTA_P80_EN	POST 80
Ref. Input	DISABLE
...	...

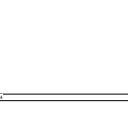
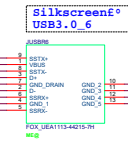
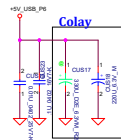
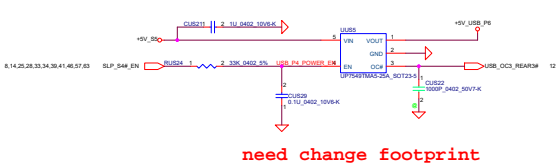
OE#	S	FUNCTION
W	X	DISABLE
L	L	D(=/-) to 2D(=/-)
L	X	D(=/-) to 2D(=/-)

Security Classification	LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	

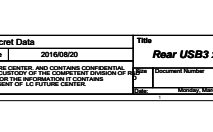
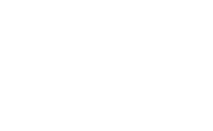
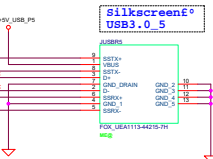
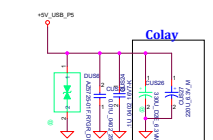
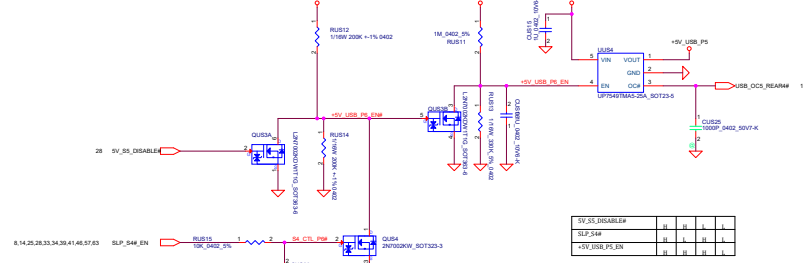
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Document Number	GB470
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3 in 1 USB3 port

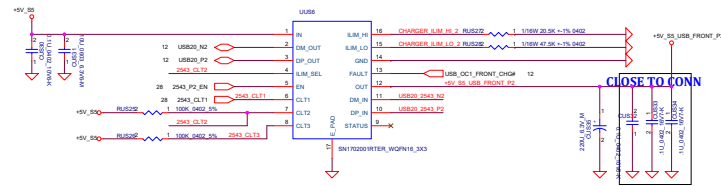


Smart power on USB

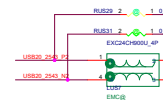
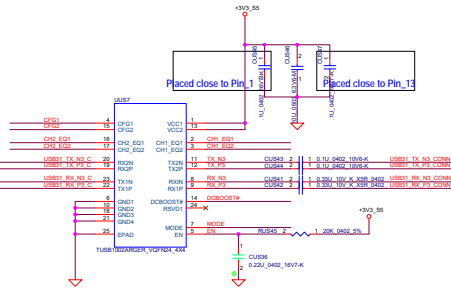


ILIM_HI	20.5K	2.5A
ILIM_LO	47.5K	1.1A

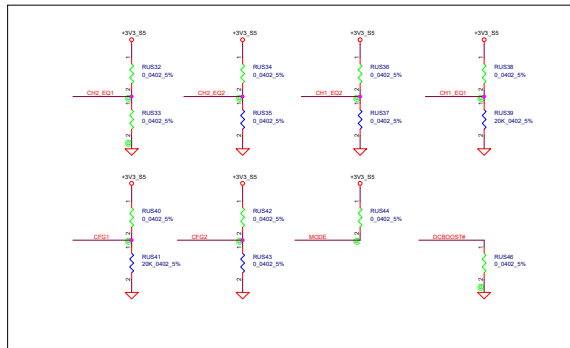
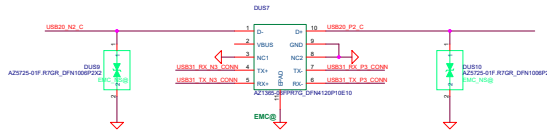
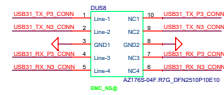
FRONT USB3.0 Charger



CLOSE TO CONN

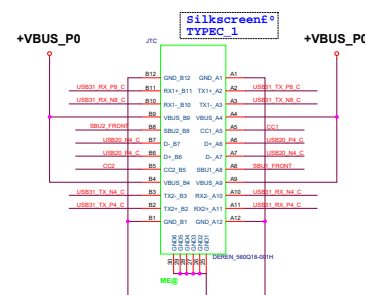
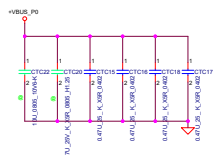


USB charge



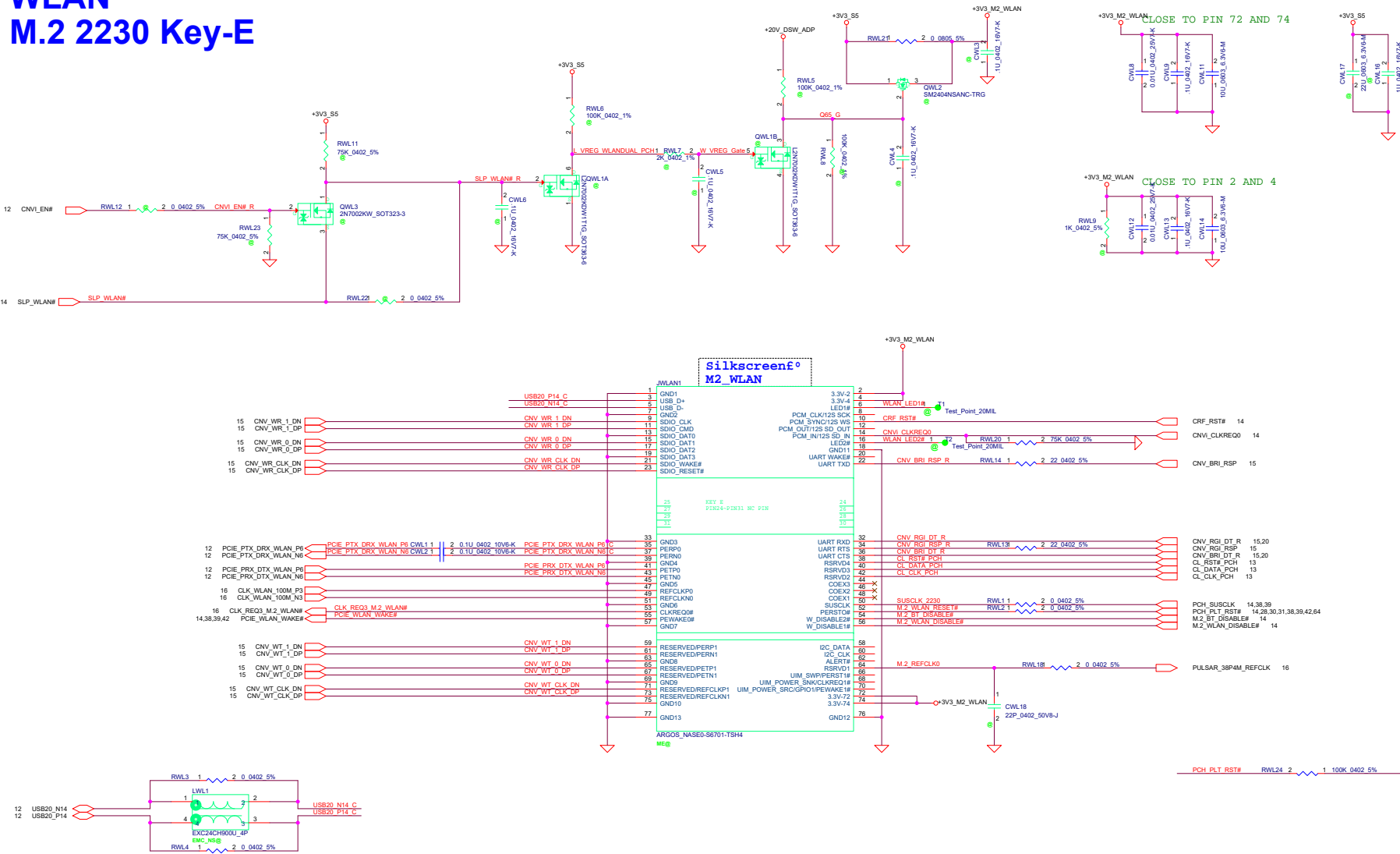
CH2_EQ2 = 0
CH2_EQ1 = F
CH1_EQ2 = 0
CH1_EQ1 = R
CFG1 = R
CFG2 = 0


CTL1	CTL2	CTL3	ILIM_SEL	Charging Mode	Current Limit Setting	TPS2543 STATUS Output (active low)
0	0	0	0	Discharge	NA	off
0	0	0	1	Discharge	NA	off
0	0	1	0	DCP / auto	ILIM_HI	off
0	0	1	1	DCP / auto	ILIM_HI ⁽¹⁾	DCP load present ⁽²⁾
0	1	0	0	SDP	ILIM_LO	off
0	1	0	1	SDP	ILIM_HI	off
0	1	1	0	DCP / auto	ILIM_HI	off
0	1	1	1	DCP / auto	ILIM_HI	DCP load present ⁽²⁾
1	0	0	0	DCP / Shorted	ILIM_LO	off
1	0	0	1	DCP / Shorted	ILIM_HI	off
1	0	1	0	DCP / Divider1	ILIM_LO	off
1	0	1	1	DCP / Divider1	ILIM_HI	off
1	1	0	0	SDP	ILIM_LO	off
1	1	0	1	SDP	ILIM_HI	off
1	1	1	0	SDP	ILIM_LO	off
1	1	1	1	SDP	ILIM_HI	off
1	1	1	1	CDP ⁽⁴⁾	ILIM_HI	CDP load present ⁽⁵⁾



WLAN

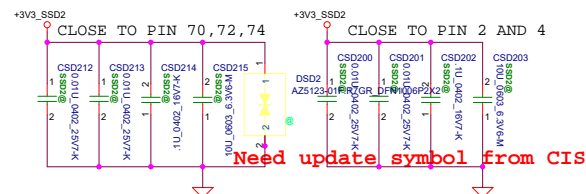
M.2 2230 Key-E



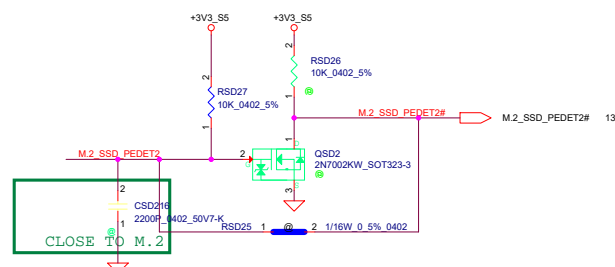
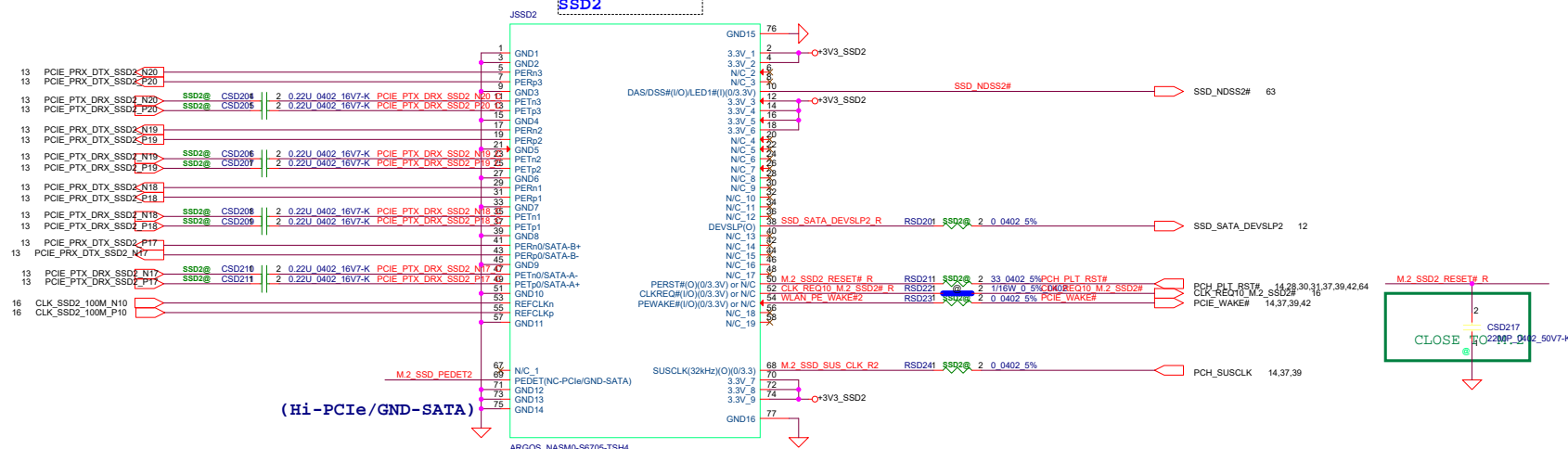
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Issued Date		2015/08/20		Deciphered Date		2016/08/20		M2 2230-E WIF/ BT/CNV					
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										Document Number		Revision	
										Date		Date	
										Date		Date	
Date: Monday, March 23, 2015										Sheet 37 of 64			

M.2 Connector SSD2#(Black)

JSSD3 on TOP Layer
JSSD2 on Bottom Layer




Silkscreen£⁰
SSD2

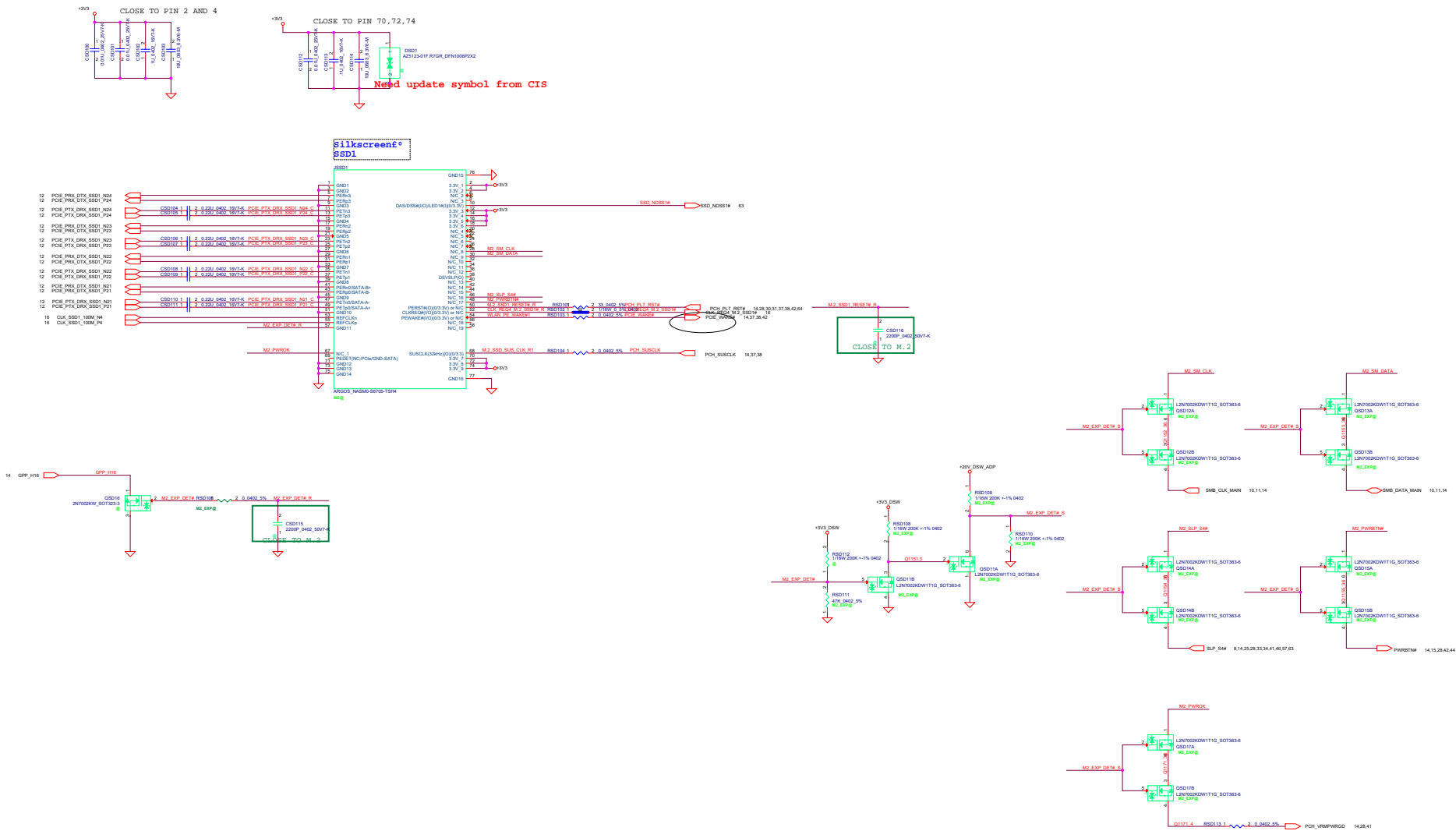



SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express® Gen 2 Only	PCI Express® Gen 3 Only	SATA Only	PCI Express® Gen 2/ SATA	PCI Express® Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ¹	None ²	None ³

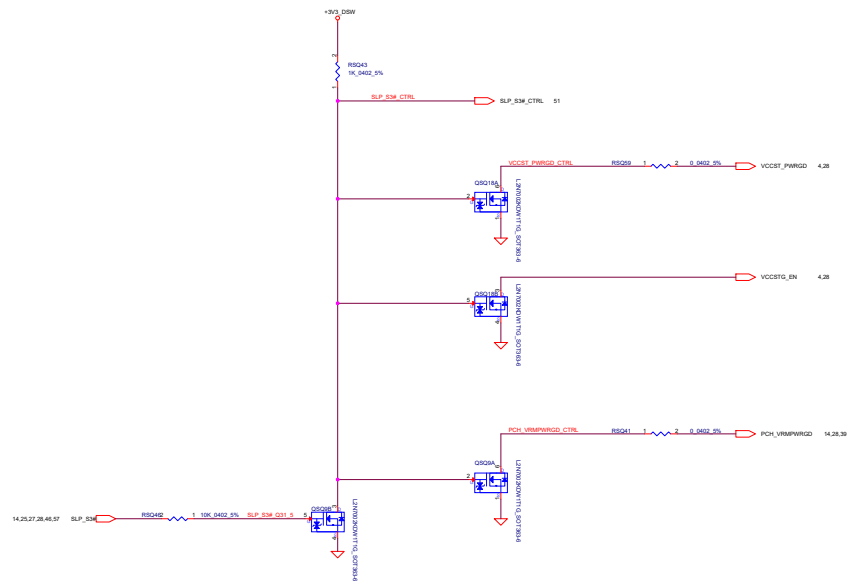
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				Document Number GH470	Rev 1.1
Date				Monday, March 23, 2020	Sheet 38 of 64

M.2 Connector SSD1#(WHITE)

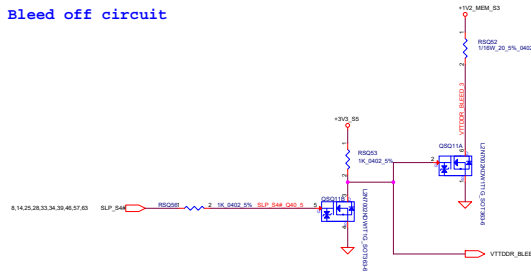


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<p>DATE</p> <p>Month</p> <p>Year</p>		<p>08</p> <p>20</p> <p>2015</p>	<p>1</p> <p>0</p> <p>0</p>

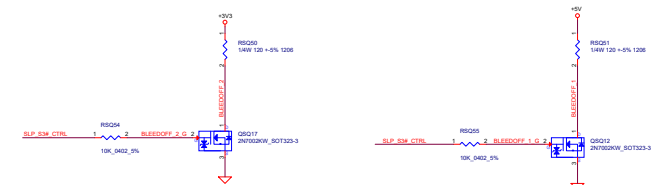




+1V2_MEM Bleed off circuit



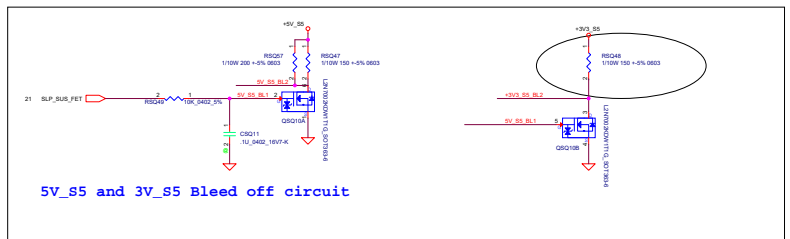
5V & 3.3V Bleed off circuit



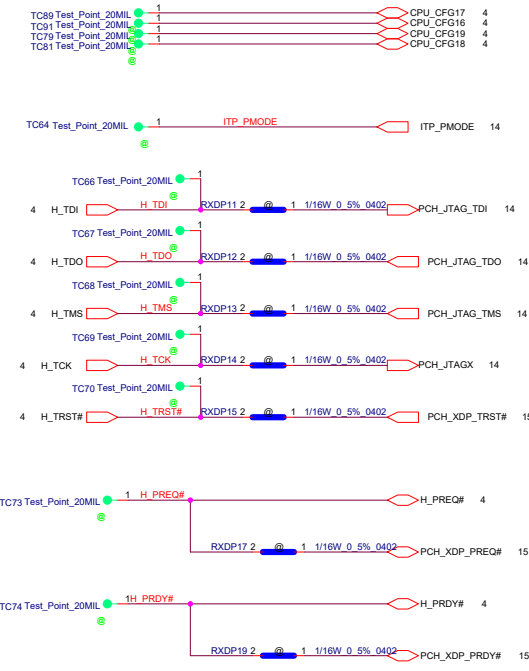
+12V Bleed off circuit

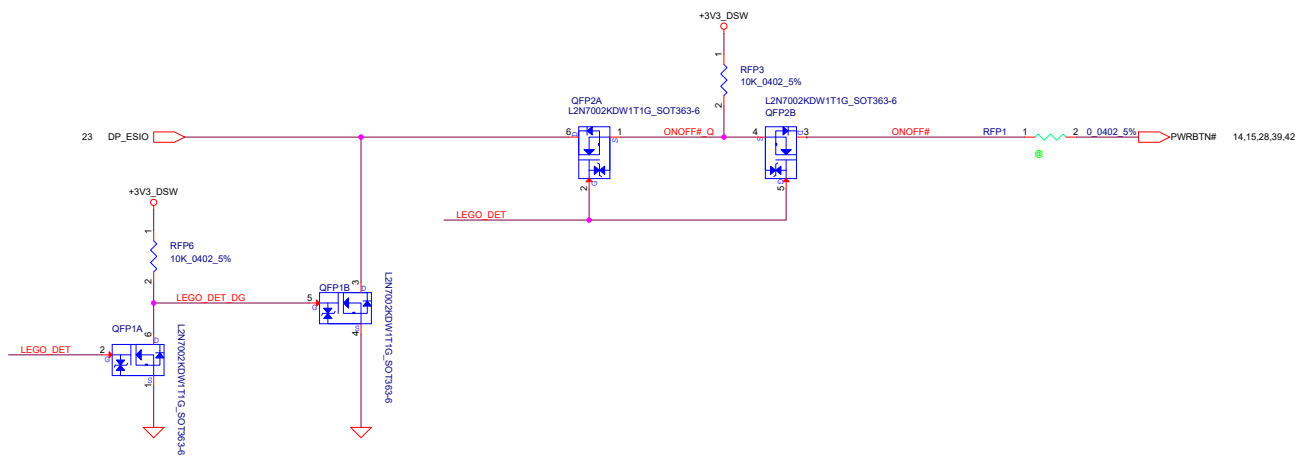
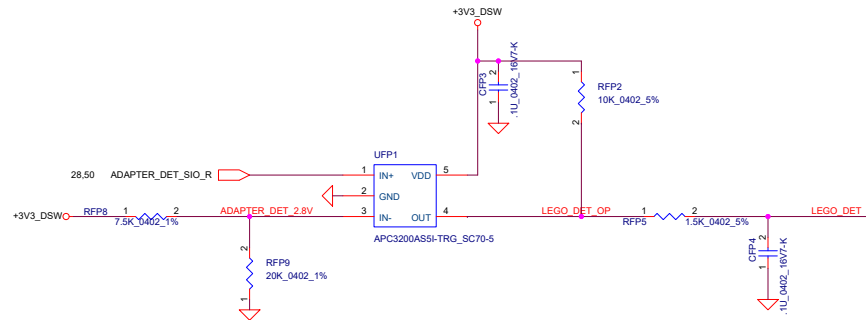
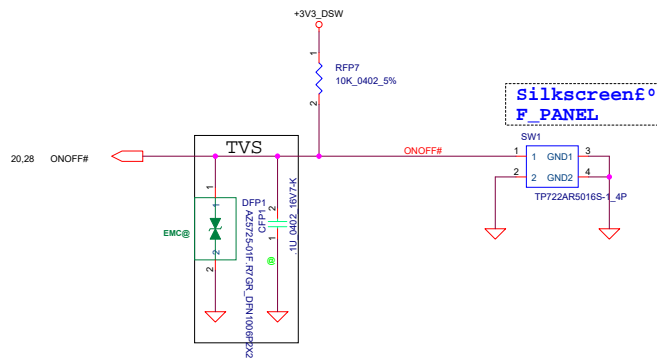


5V_S5 and 3V_S5 Bleed off circuit



Intel XDP Debugging Connector

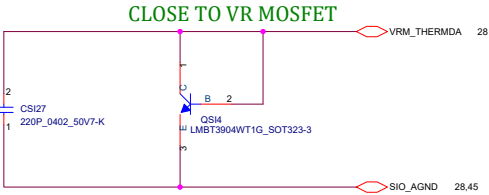




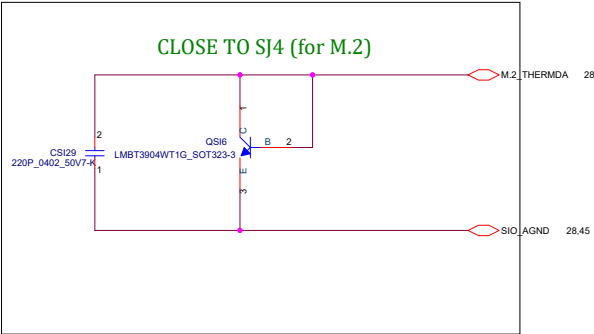
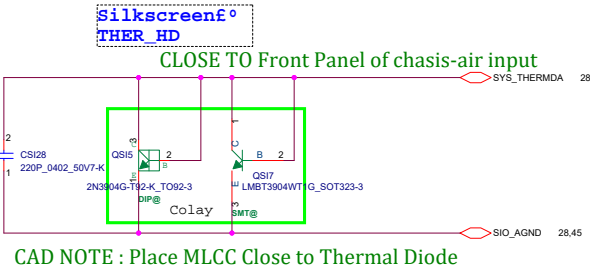
Security Classification		LC Future Center Secret Data		Title	
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				GH470	
Date				Monday, March 23, 2020	Sheet 44 of 64

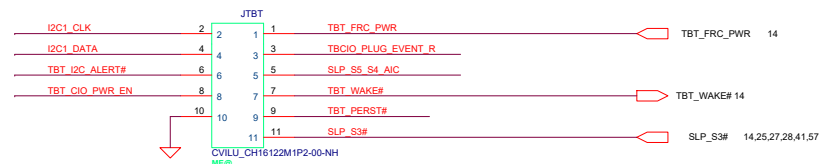
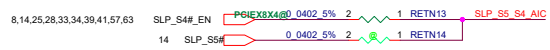
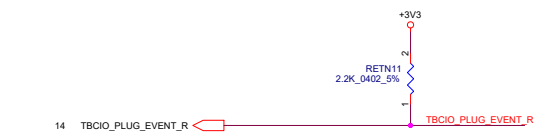
Temperature Sensing

Current Mode

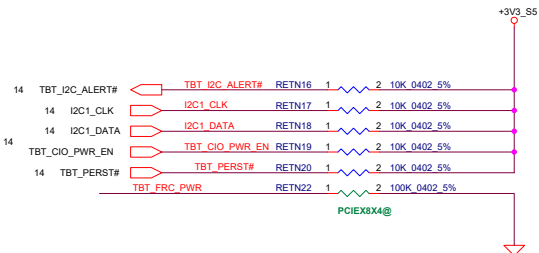


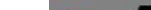
Acceptable Transistor Component
ST Micro: MMBT3904
ON Semiconuctor: MMBT3904LT1
Fairchild Semiconductor: MMBT3904FSCT

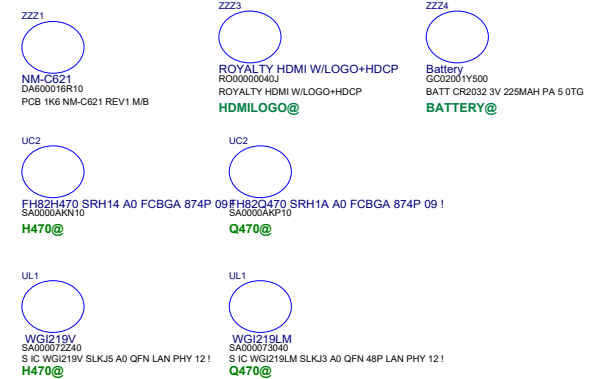
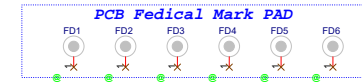
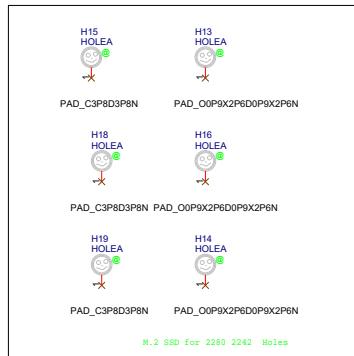
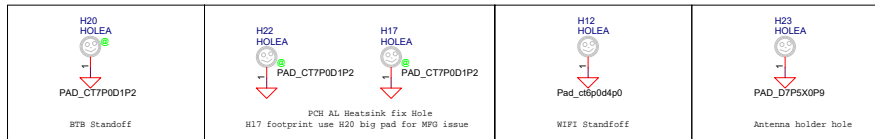
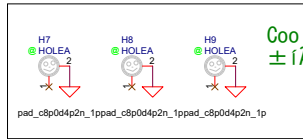
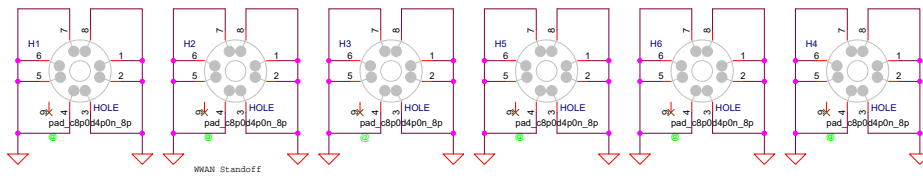




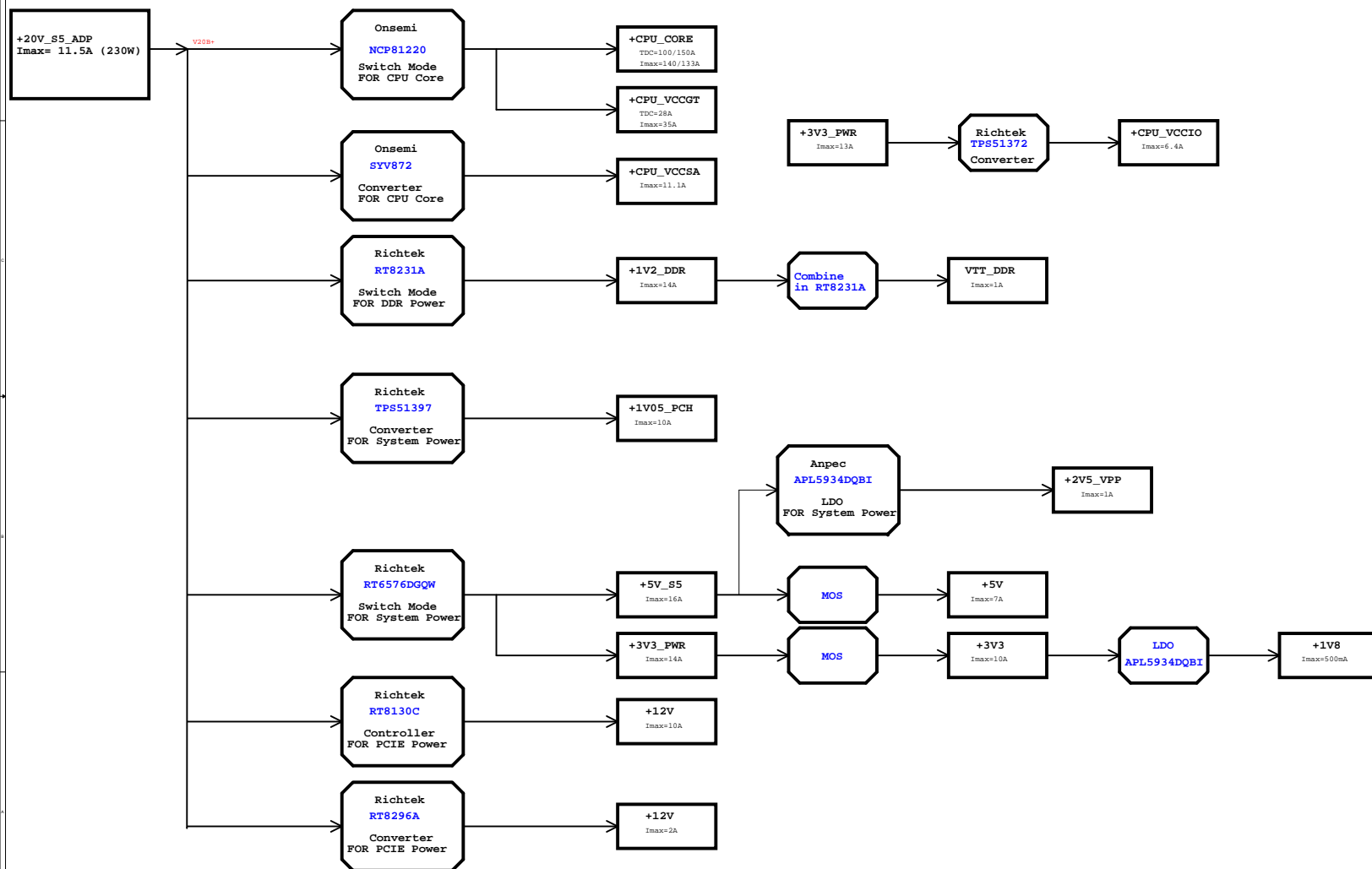
Silkscreen
TBT-HDR

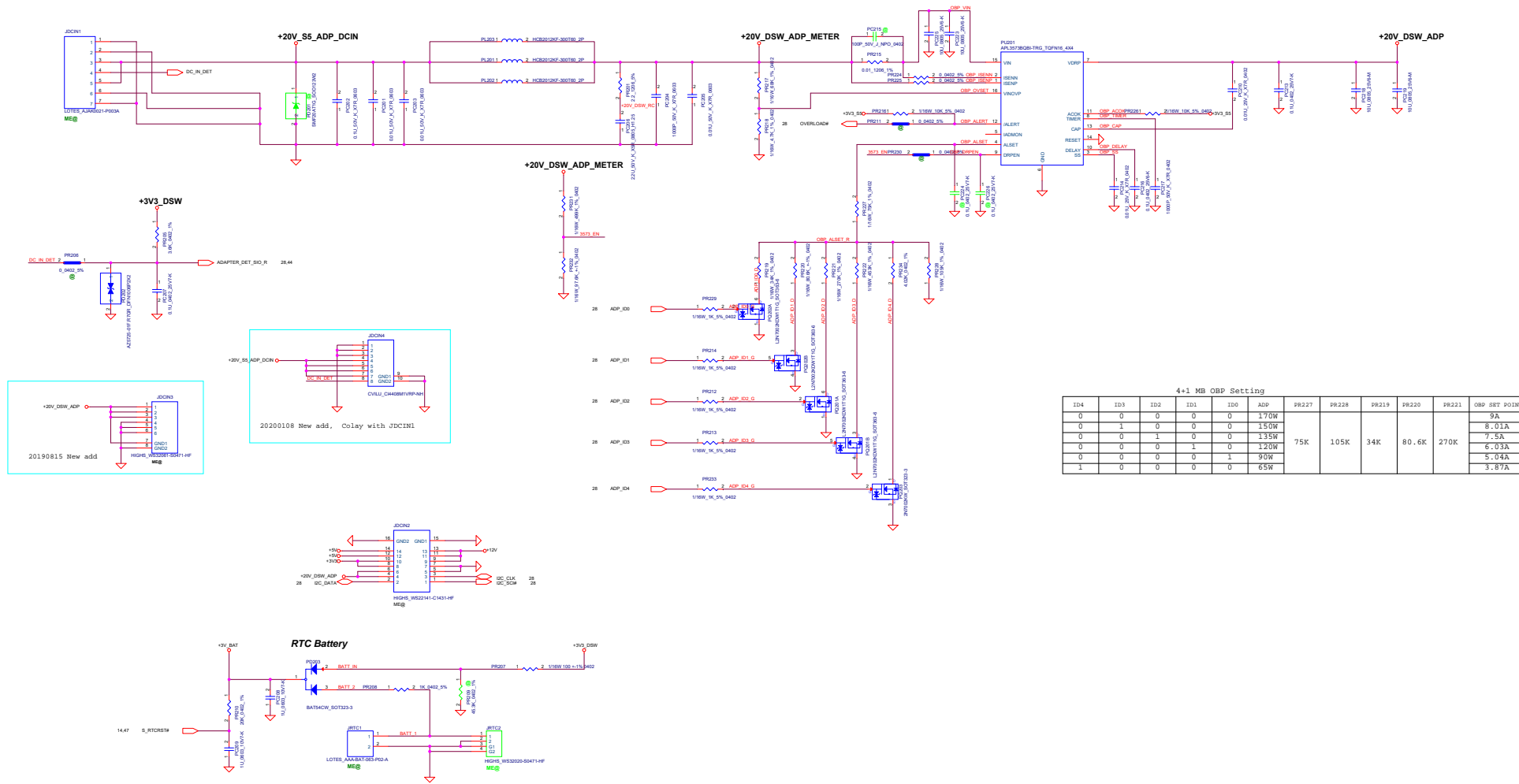


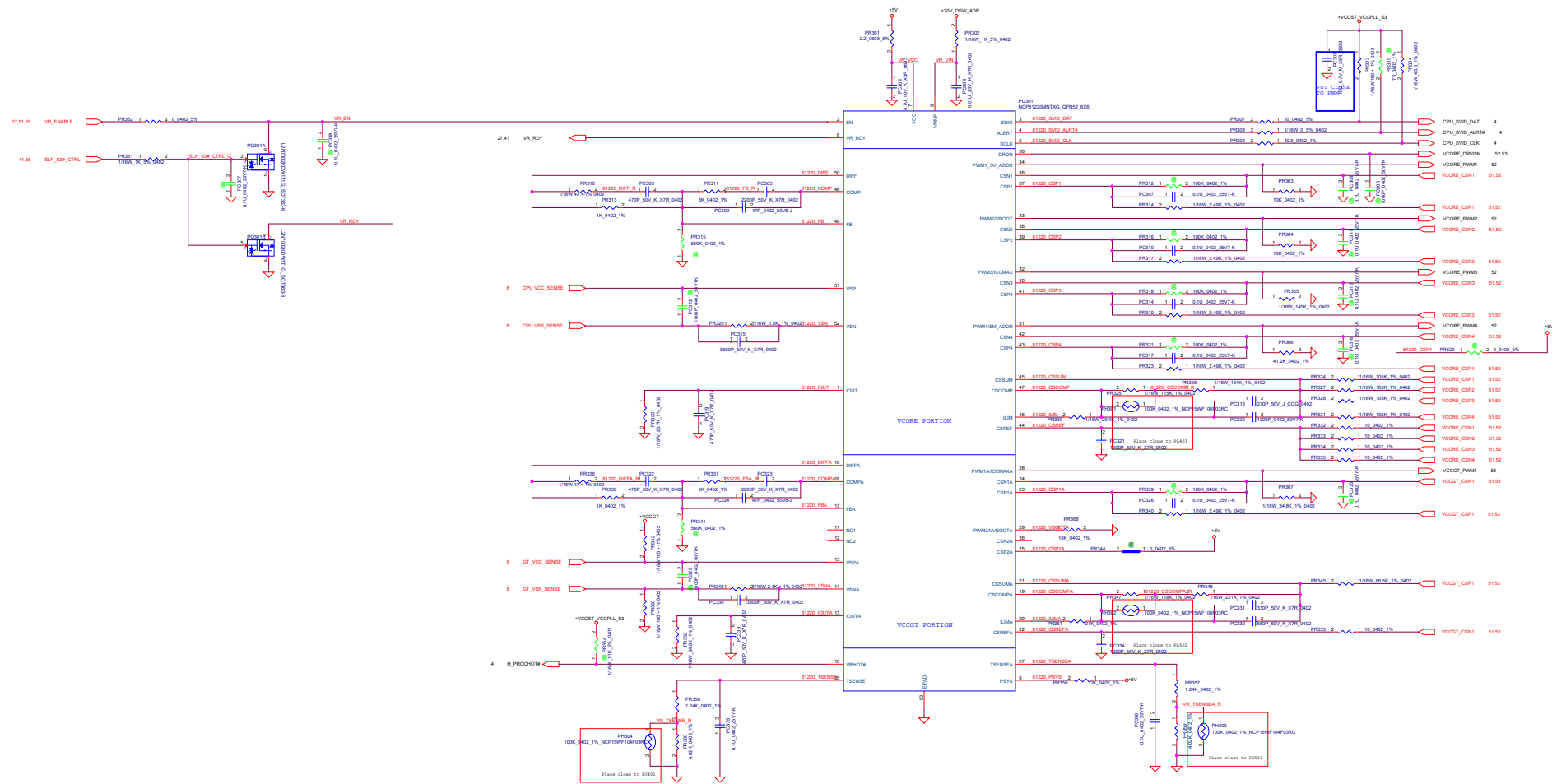
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Issued Date	2015/08/20	Deciphered Date	2016/08/20	APS	
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				Date Monday, March 23, 2020	Rev 1.0
				Sheet 47 of 64	

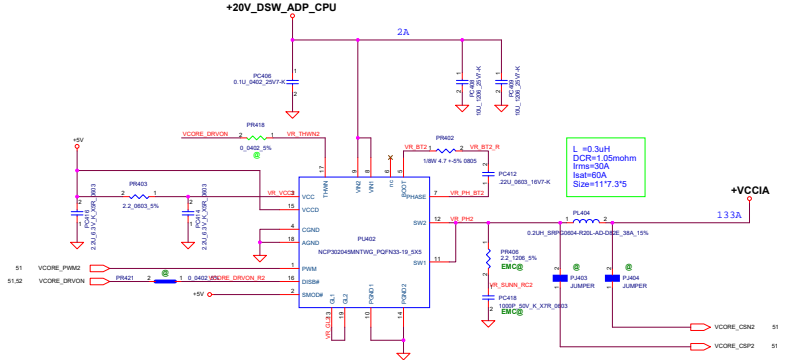
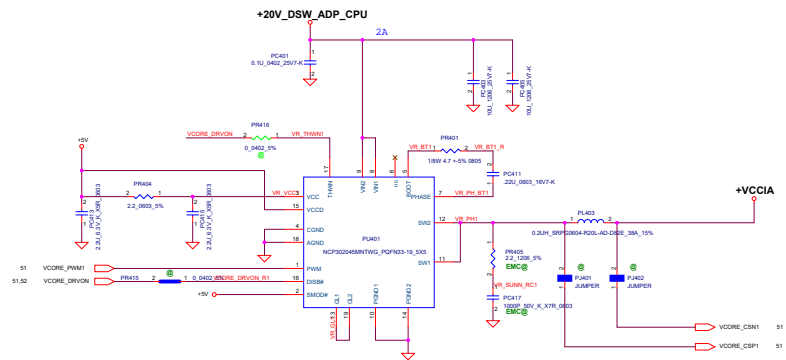


M80Q (32M)	SOP8	USP1 MX25L25673GM2I-08G SOP 8P SPIROM1@
M70Q (16+8M)	SOP8	ZZZ2 WINBOND 16+8 X7649W09001 Tiny6 GH470 4+1 MB WINBOND 16+8 SPIROM2@

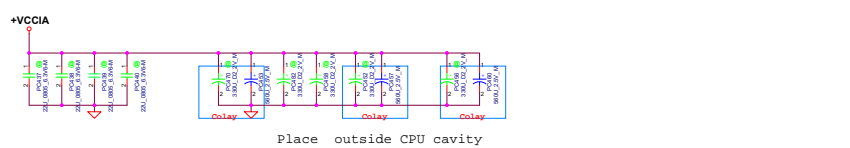
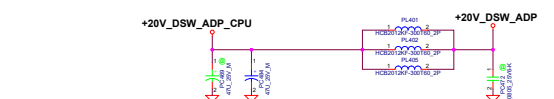
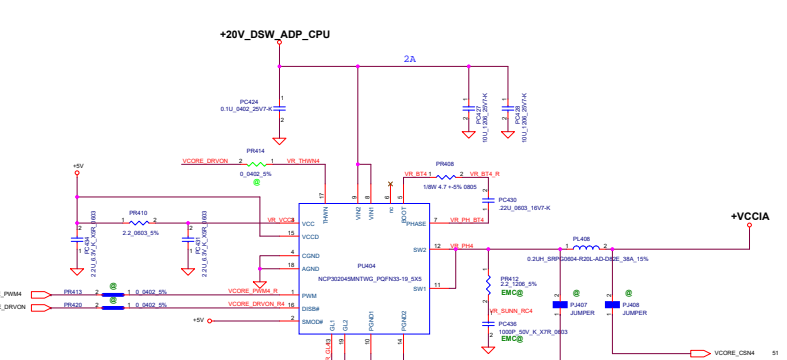
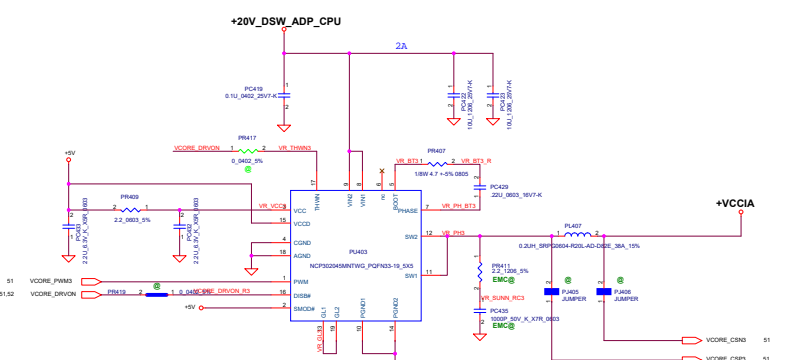




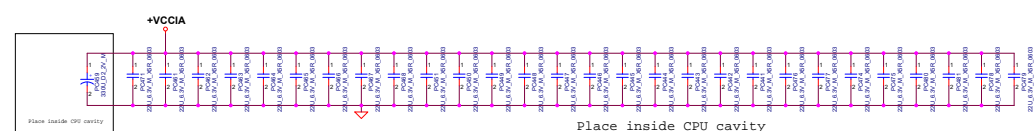




VID=0 V-1.52 V
 Vboot=0V
 DCR=1.05mohm
 IIR=33%
 TDC/ICmax=91/133A
 OCP=150%~200%
 OVP=Vout+200mV
 UVP=Vout-300mV
 Fsw=400KHz
 Vin_rms =9.7A
 MLC ripple current = 7.6A
 Cin_CAP =187uF
 Cout_CAP =2633uF

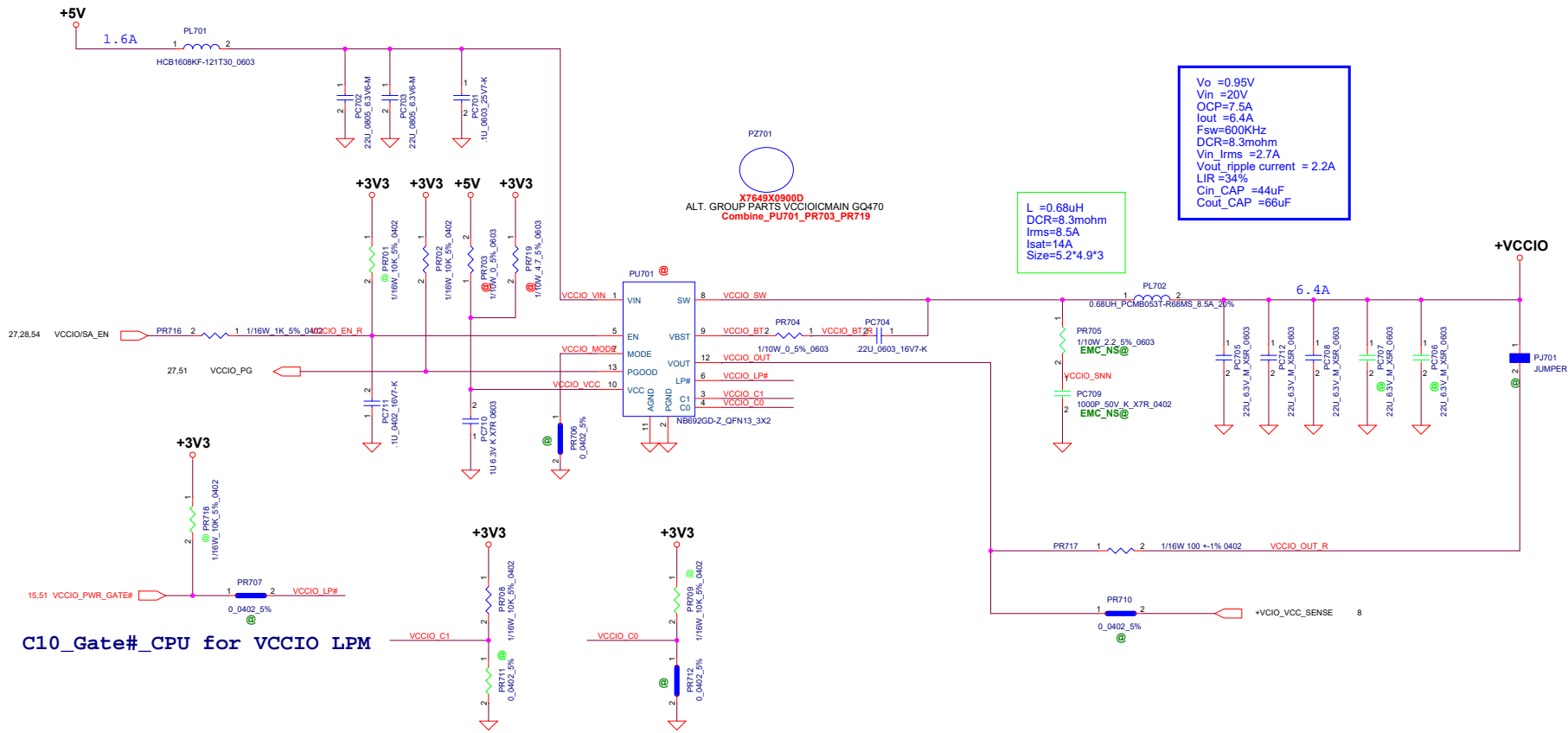


Place outside CPU cavity

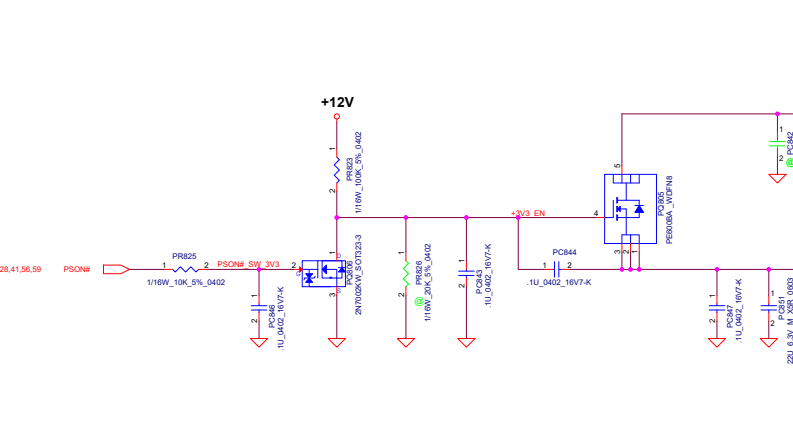
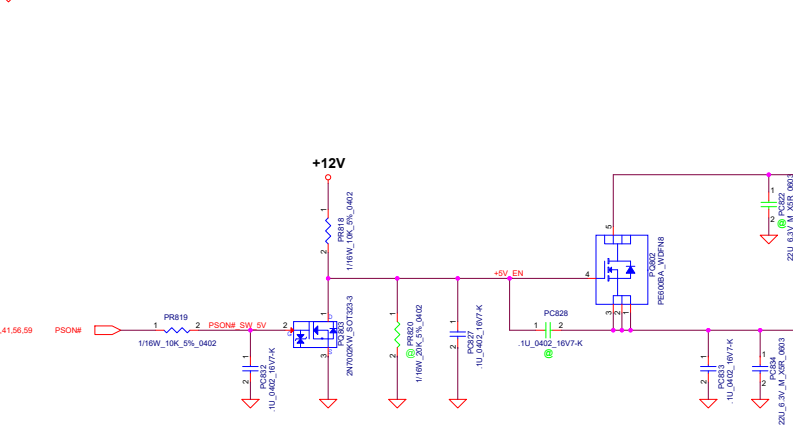
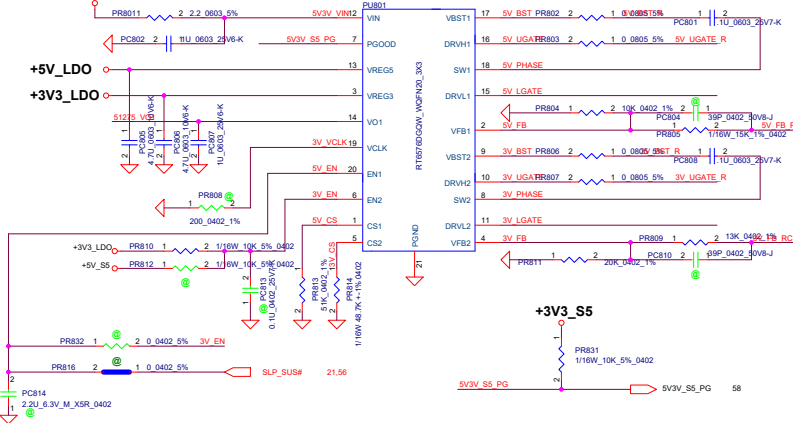


Place inside CPU cavity

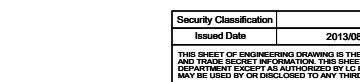
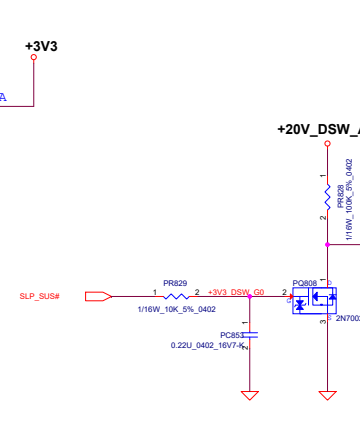
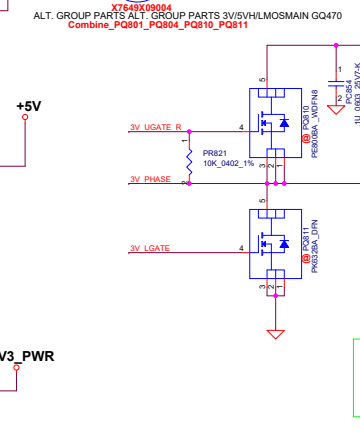
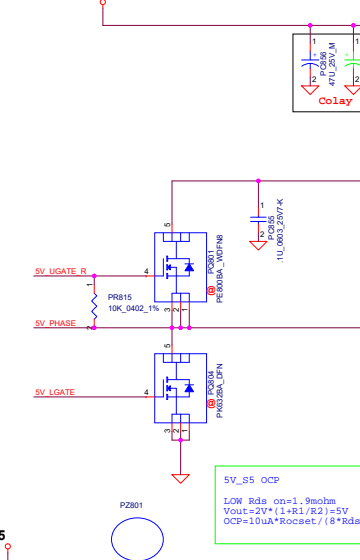
Security Classification	LC Future Center Secret Data		Title
Issued Date	2013/08/08	Deciphered Date	2013/08/08
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90490			0.1



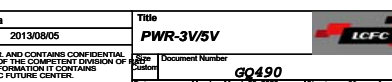
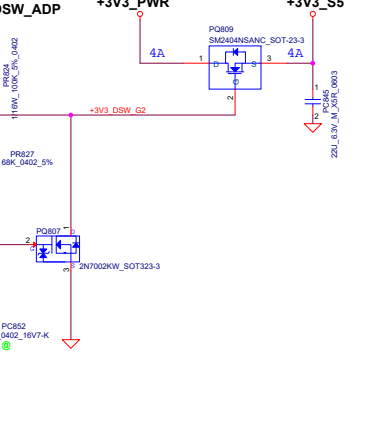
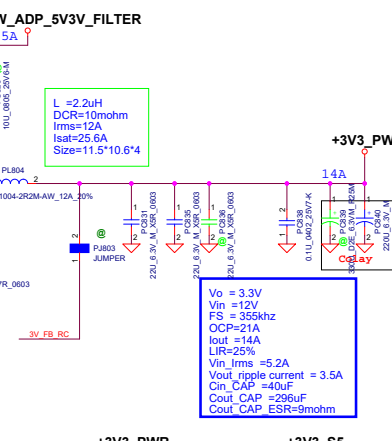
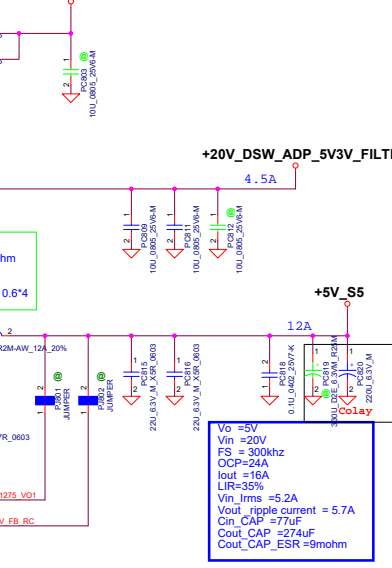
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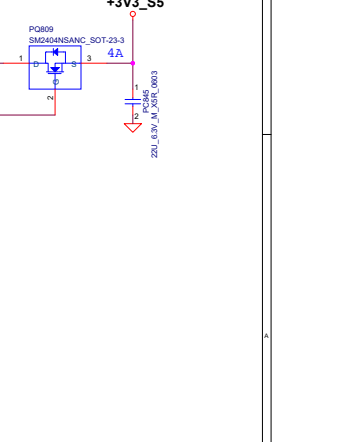
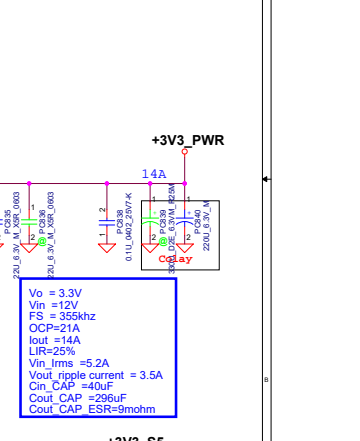
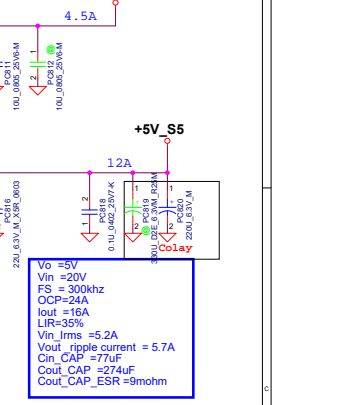
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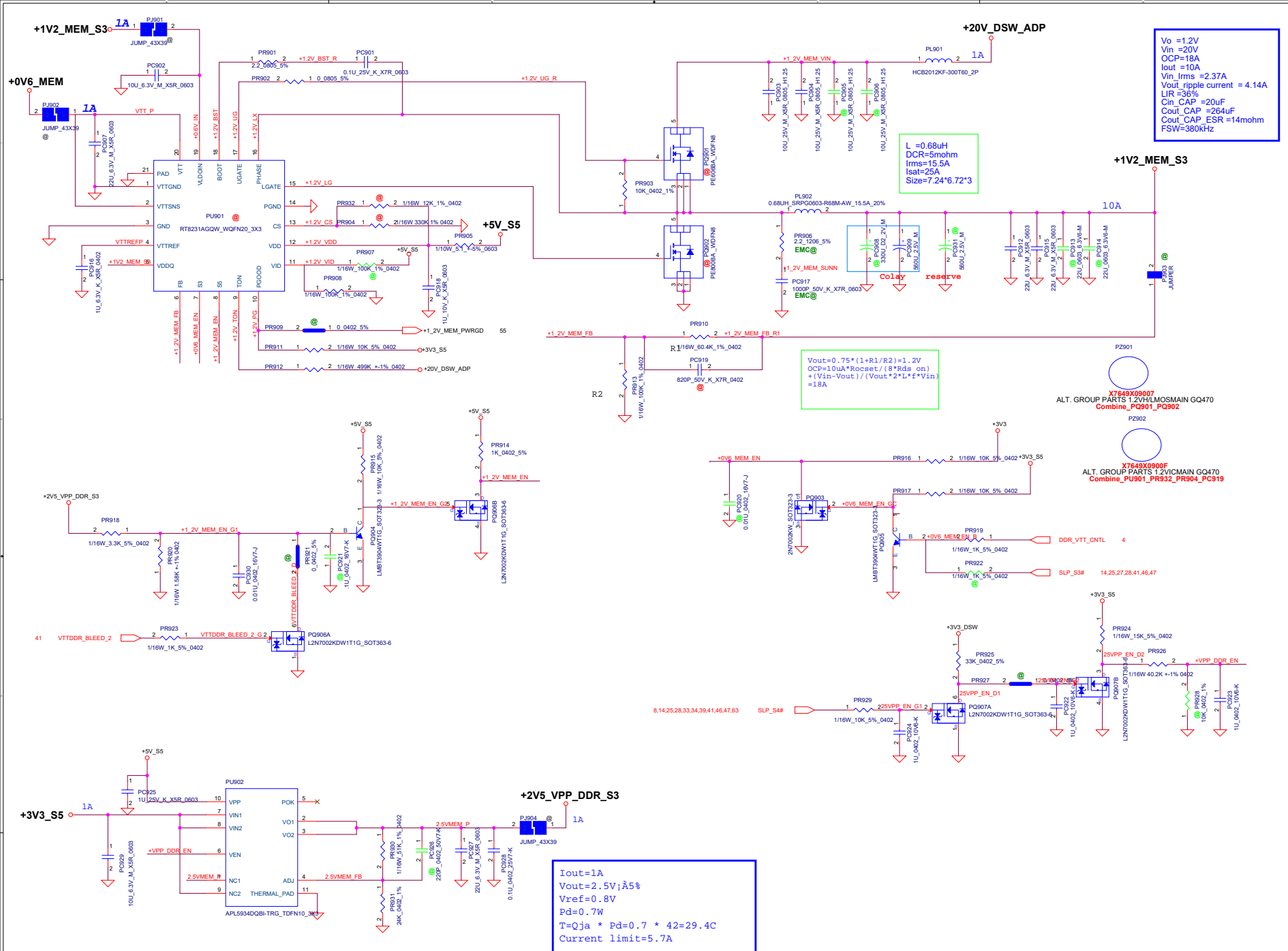
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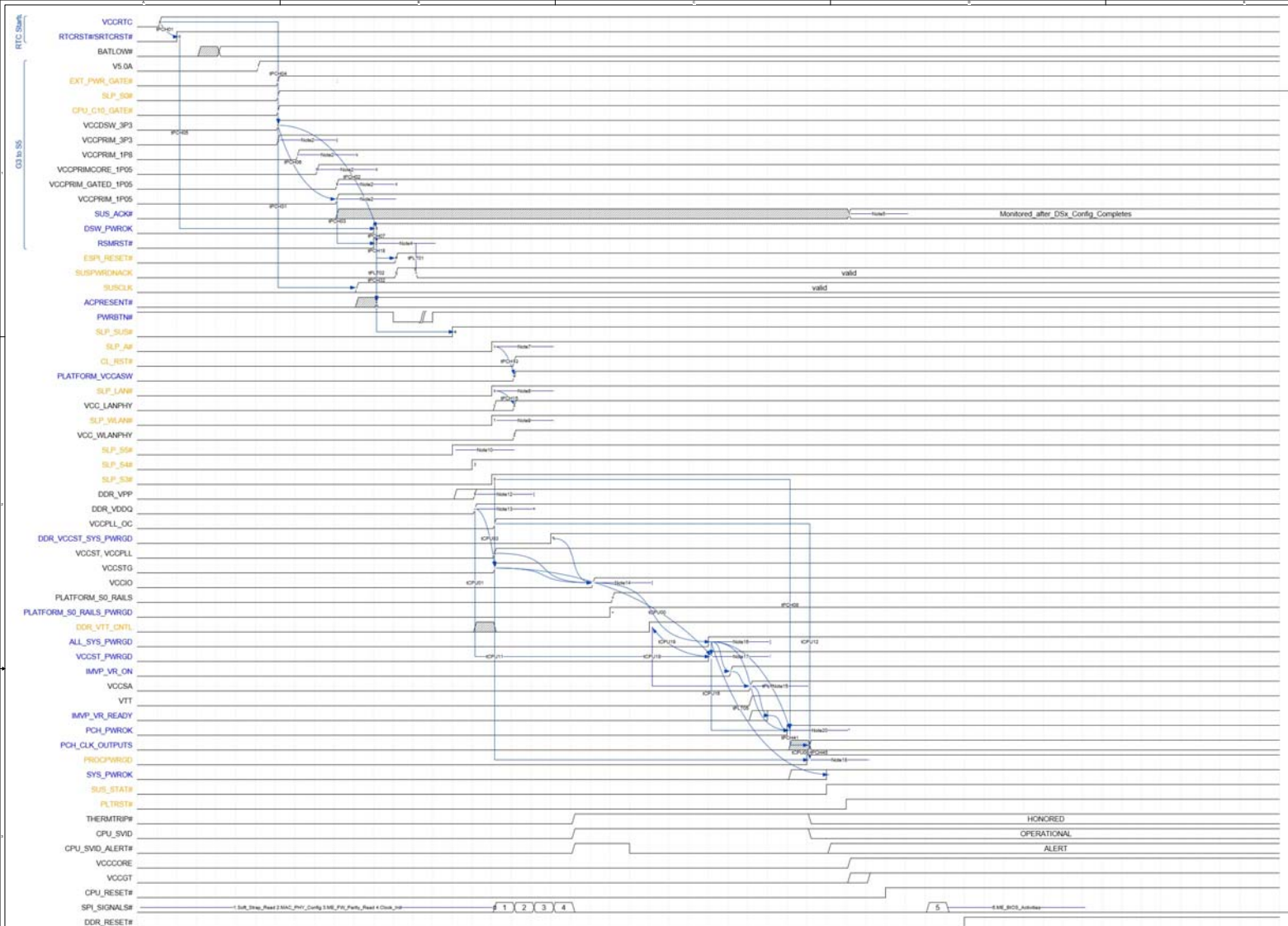


+20V_DSW_ADP_5V3V_FILTER



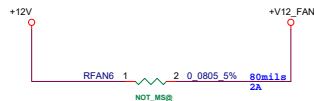
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	
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Document Number				Q490
Date				Monday, March 25, 2008 15:00 56 of 64





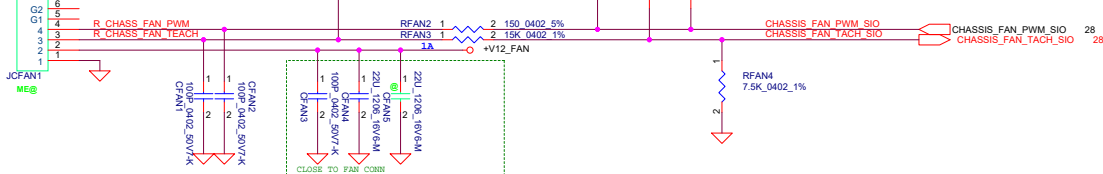
with Deep Sx support

source	destination		G3	DEEP S5	S0
board	PCH	VBAT			
board	PCH	RTICRST#			
PSU	board	+5VSB_DSW			
board	PCH	+3VSB_DSW			
board	PCH	PCH_DPWROK			
PCH	SIO	PCH_SUSWRN#			
SIO	PCH	PCH_SUSACK#			
PCH	SIO	SLP_SUS#			
board	board	+5V_S5			
board	PCH	+3V3_S5			
board	PCH	+1V0_PCH			
SIO	PCH	RSMRST#			



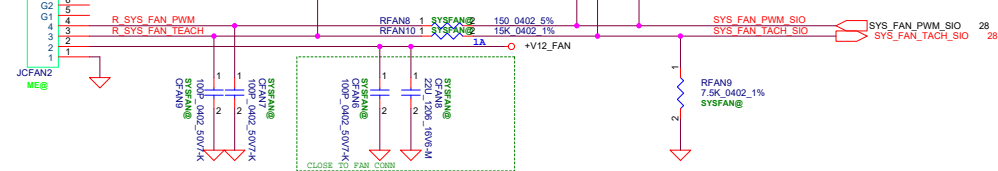
Silkscreenf°
CPUFAN1

HIGHS_WS32040-S0471-HF

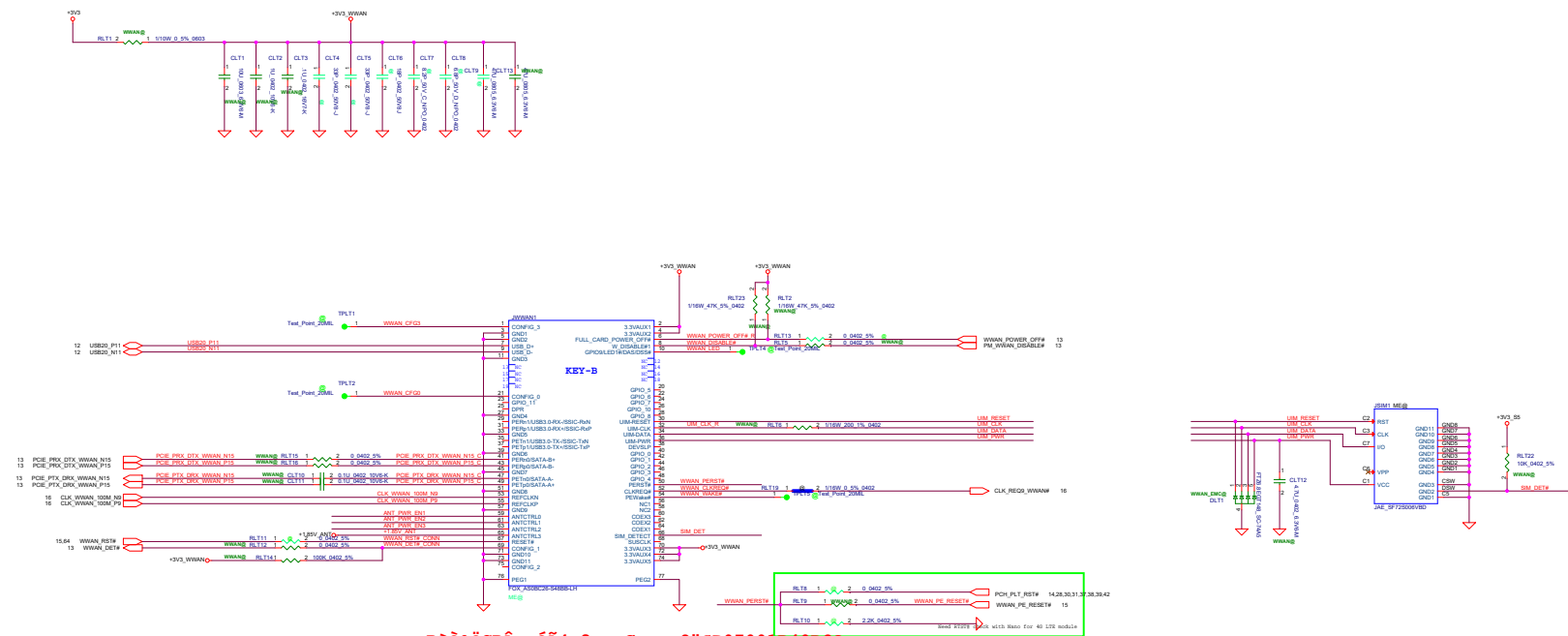


Silkscreenf°
CPUFAN2

HIGHS_WS32040-S0471-HF



TYPE-B NGFF LTE CARD FOR WWAN

[illegible]